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Fabrication of Thin Film Nanoscale Alumina Templates

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Thesis

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Abstract

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Semiconductor nanostructures have superior electronic and optical properties that are expected to play an important role in 21st century electronic and photonic devices. Recognizing this potential, semiconductor nanostructures have been the focus of research over the past 25 years, and many ultra-high performance devices have been demonstrated. While the potential of this class of devices is clear, their commercial applications have been limited by the lack of a fabrication process suited to economical volume production. The initial method of nanostructure fabrication using electron beam lithography and reactive ion etching is not considered practical due to its high cost and low throughput. The technologies that are considered serious candidates are the nanogrowth techniques where the semiconductor material is synthesized in the size and the shape of the nanostructures. Most of these techniques, however, do not provide any control over nanostructure size and periodicity which are important requirements for device applications.

We have developed a nanostructure fabrication technique that provides excellent control over device size and periodicity, and is appropriate for low cost commercial manufacturing. This technique uses electrochemical synthesis of semiconductor nanostructures in a preformed alumina (Al_2O_3) template. The template is created by electrochemically etching, or anodizing, a thin layer of aluminum deposited on a silicon or a glass substrate. When aluminum is anodized, a two dimensional periodic network of Al_2O_3 cells with uniform tubular pores is formed, the diameter of which can be precisely varied between 4 nm and 100 nm by controlling the anodization conditions. The semiconductor nanostructures are then created by electrochemically depositing the material inside the pores. This thesis will provide details about the fabrication technique of the template as well as experimental results for optimization of the fabrication technique.

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I would like to give special thanks to my advisor Dr. Das for his guidance, expertise and encouragement to pursue this research. Special thanks also go to my committee and the faculty and staff of the department. Their expertise and tutelage have been invaluable to my success. I would also like to thank Stephen McGinnis, my partner in crime, for his theoretical knowledge, guidance, ideas and new angles to try. Thanks go out to Chris Garman for spending the time sculpting the Teflon apparati. I would also like to thank Kolin Brown for showing me how to use the fabrication equipment in the fabrication lab when I first started this research. And finally thanks to my friends and family who have supported me throughout my education.

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1. Introduction

The development of low dimensional semiconductor nanostructures has been the focus of research and development over the past 25 years due to the enhancement in electronic and optical properties which occurs when electrons are strongly confined in one, two or three dimensions. The commercial value of this class of technology can be seen in the widespread use of semiconductor lasers and high electron mobility transistors based on quantum confinement in one dimension (quantum wells). However, it has been theoretically [1-3], and experimentally [4-7], demonstrated that semiconductor quantum wires and quantum dots, where electrons are confined in two and three dimensions respectively, can provide significant further enhancement of device performance. In addition, these low dimensional structures emit and absorb light in an extremely narrow spectral range which can be controlled by the shape, size, composition, and doping of the nanostructure [8]. These effects have recently been exploited to fabricate preliminary quantum dot lasers [9-11].

While the potential of semiconductor nanostructures is clear, their applications have been limited by the lack of a fabrication process suited to economical volume production. The common method of nanostructure fabrication uses electron-beam lithography to define the structures on a Molecular Beam Epitaxy (MBE) grown film which are then etched using Reactive Ion Etching (RIE) [2]. However, due to the serial nature of e-beam lithography, this method is not suitable for the fabrication of large arrays of nanostructures needed for most practical applications. In addition, this technique has been shown to cause process related damage which can significantly degrade device performance [12]. This has led to the development of a number of ‘nanogrowth’ techniques where the semiconductor material is synthesized in the size and shape of a quantum wire or a dot. Strain-induced epitaxial growth [13], and chemical synthesis in glass dielectric matrices [14] can produce large arrays of semiconductor nanostructures in the required

size range (1-100 nm), although these techniques lack the desired control over device size and periodicity [15]. Capped colloidal nanostructures have been fabricated with great success for experimental investigations of basic electronic and optical processes in nanostructures [16]; however, since the resulting quantum dots are suspended in a liquid solution, their practical applications are uncertain due to packaging and reliability problems. Therefore, there is a need for a process to economically fabricate large periodic arrays of semiconductor nanostructures that will allow (a) the size and composition of the nanostructures to be varied, (b) encapsulation of the semiconductor nanostructures in a rugged host material, (c) flexibility to use a variety of substrate materials, and preferably, (d) compatibility with standard silicon CMOS fabrication techniques.

The Nanostructures Research Group at West Virginia University has developed such a technology for the electrochemical fabrication of large, periodic arrays of semiconductor nanostructures. The technique uses material growth on a preformed template formed by electrochemical etching (anodization) of a thin film of aluminum deposited on an arbitrary substrate. The template contains a periodic array of pores in which the nanostructure materials are synthesized. The nanostructure size and periodicity can be controlled by controlling the anodization conditions. The technique is inexpensive, reliable, suitable for the fabrication of a variety of semiconductors, and compatible with the standard CMOS process. We are currently using this fabrication technique to develop a variety of different optoelectronic devices.

The objective of this thesis was to develop the process technology for the fabrication of thin film alumina templates on Silicon as well as other substrates. A particular emphasis of this thesis was to develop an empirical understanding of the pore formation mechanism in order to develop more control over template parameters. The rest of the thesis is organized as follows. Chapter two will present a description of the anodization process for bulk as well as thin film aluminum. Chapter 3 will summarize the evolution and development of the anodization apparatus used in this research. The experimental details and results for template fabrication on various

substrates will be described in Chapter 4. Chapter 5 will summarize the conclusions of this research and suggest recommendations for future work.

2. Process Development For Thin Film Templates

2.1 Anodization of Aluminum

Aluminum oxidizes naturally in the atmosphere to form a very thin layer of aluminum oxide coating, Al_2O_3, which adheres strongly to the metal's surface, protecting it from further reaction. A thicker layer of Al_2O_3 can be produced by immersing the Aluminum in an electrolytic solution and passing an electrical current through it, similar to electroplating. This process of electrochemical oxidation is also known as anodization. The protective oxide coating on aluminum is frequently enhanced by the process of anodization for coloring and anti-corrosion applications. An interesting feature of anodized alumina is that is contains a two dimensional hexagonal lacework of cells with uniform tubular pores. The pore diameter and the cell wall thickness depend on the anodization conditions, such as type and pH of anodizing acid, and the anodizing current density, and can be precisely controlled over a wide range. Pore diameters can range from 4 nm to 200 nm, pore length from 10 nm to 1000's of nm, with pore density in the 10^9 - 10^{11} cm^{-2} range [17-27]. In recent years, researchers have reported self-organized pore growth leading to a nearly perfect, densely packed hexagonal pore structure for a narrow set of processing parameters [28-35]. A systematic investigation by Jessensky *et. al.* suggests that the cause of this self-ordering behavior is mechanical stress which leads to a repulsive interaction between neighboring pores [31].

Although the anodization process has been around for years, the pore formation mechanism is not yet fully understood. The structure was first characterized by Keller, Hunter, and Robinson [36] as a close-packed array of columnar hexagonal cells each containing a central

pore normal to the substrate surface. This characterization is known as the Keller Model and is schematically shown in Figure 2.1, It is also called the Hexagonal Column Model. A similar model was also proposed by Akahori[37]. Another model was proposed by Murphy and Michelson [38], who studied sulphuric acid films chemically and reported that the cells and barrier layers are composed of hydrous and hydrated oxide particles. They reported the structure of oxide film as an aggregate of colloidal particles of aluminum compounds as shown in Figure 2.2. The surface of the oxide film has colloids with high water content, and the inner layer of the film is an aggregate of colloidal particles with low water content. The Murphy Model is also referred to as the "Colloidal Model."

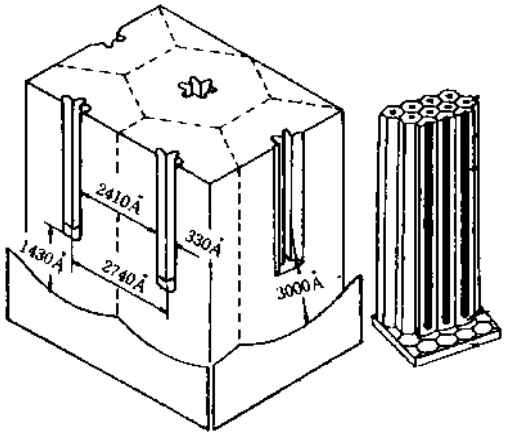

Figure 2.1 Schematic of the Keller model

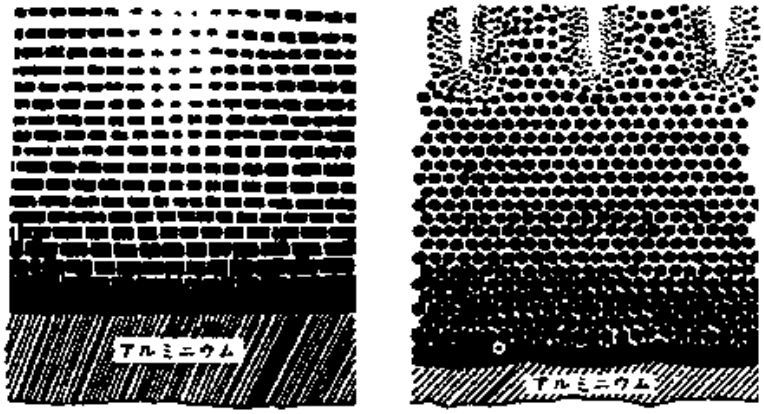

Figure 2.2 Schematic of the Murphy Model

Thompson [39, 40], Takahashi [41] and Fukuda [42] proposed new models constructed from cells and barrier layers, having inhomogenous chemical compositions. These models termed the Wood Model is shown in Figure 2.3. The bold black-line part of the Wood Model is a fine oxide layer that does not contain electrolytic anions, and the aggregate of black circles shown in the figure is an oxidized aluminum colloidal layer containing a large number of electrolytic anions. Wood's Model was proposed based on observations of oxide film using an electron microscope and results of tests of instrumental analysis. The Wood Model is said to be a compromise between the Keller Model and the Murphy Model.

Although the chemistry of the pore formation mechanism has not been fully established yet, the anodization process is believed to take place in the following steps. Anodization can be carried out under constant voltage or constant current conditions. We will assume constant current anodizations for this section. A convenient way to monitor the anodization process is to measure the voltage time characteristics. Figure 2.4 shows a typical voltage time characteristic curve for the anodization of bulk aluminum. During the first 3-5 seconds of anodization, a thin non-porous layer of alumina (Al_2O_3) is formed on top of the aluminum layer as indicated by the

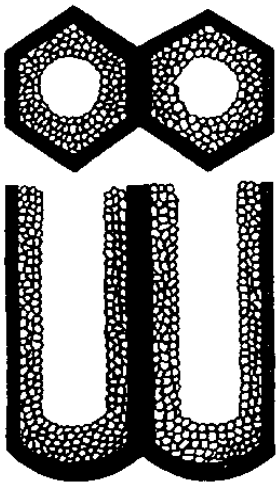

Figure 2.3 Schematic of the Woods model

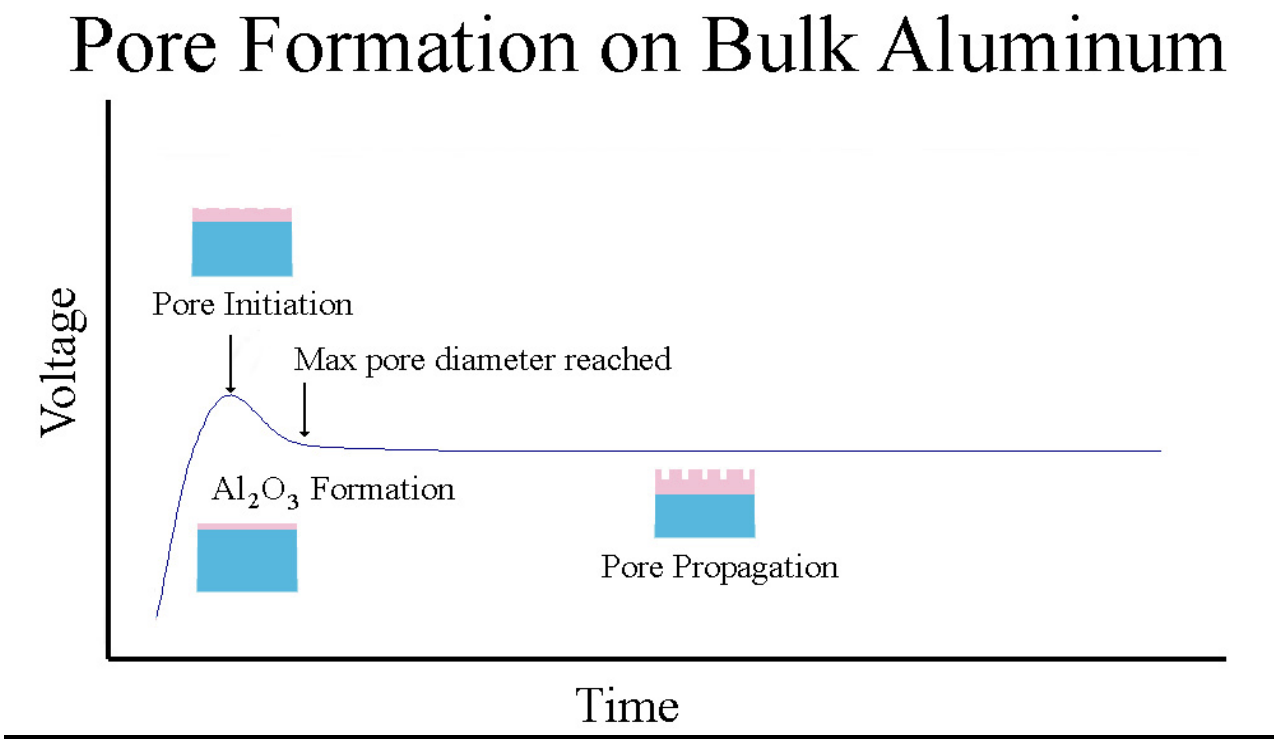

Figure 2.4 Voltage time characteristics during anodization of bulk aluminum

rise in potential. As the anodization is continued, an array of pores develop on the alumina layer, and grow in diameter until reaching the final dimension determined by the anodization conditions. This is indicated by a decrease in potential which reaches a final steady state value once the final pore diameter is reached. Once the final diameter is reached, the diameter of the pores do not increase any further. The depth of the pores increase in proportion to the anodization current as the anodization is continued.

Although the anodization of bulk aluminum has been investigated quite extensively, it is not appropriate for practical device applications due to the thick layer of unreacted aluminum underneath. We have extended this previous research by developing a technique to perform this anodization on a thin film of aluminum deposited on an arbitrary substrate. This approach provides the possibility of nanostructure integration on silicon substrates, and provides us with a tool for precisely controlling the nanostructure depth by monitoring the voltage-time characteristics during anodization. Voltage time characteristics durign the anodization of a thin film of aluminum is shown in Figure 2.5. During anodization, the potential increases initially during the formation of the top layer of Al_2O_3, then decreases during pore widening, and then levels off at the onset of pore propagation. Next, when the pores propagate through the complete layer of aluminum film, and contacts the silicon substrate, the potential rapidly increases. Since the thickness of the aluminum film is accurately known, and the time from the beginning to the end of pore formation can be determined from the potential profile, the pore formation rate can be precisely determined in this system. Therefore, in addition to providing control over the diameter of the pores, our approach also provides precise control over the *length* of the pores.

The objective of this thesis was to investigate the template formation process to gain control over template parameters. We have successfully created thin film templates on aluminum substrates, silicon substrates and glass substrates and have achieved a pore diameter variation of within ± 10%, the results of which are presented in the next few chapters.

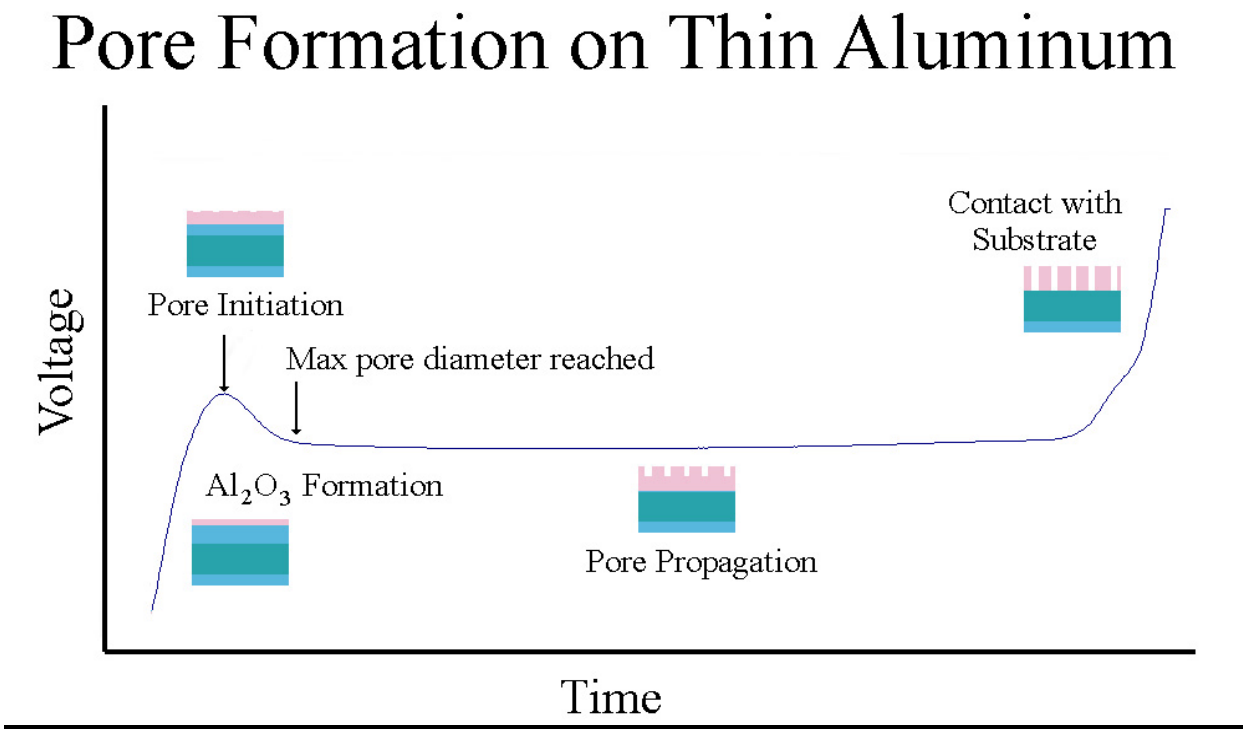

Figure 2.5 Voltage Time characteristic during anodization of Aluminum thin film on Silicon

3. Evolution of Anodization Apparatus

Several apparatuses have been tried throughout this research in an effort to find the most feasible and the simplest design. The first apparatus tried was a large area anodization apparatus. This apparatus could handle 3" wafers and would anodize a 2 ½" diameter area. The sample was also designed to be put at an angle to allow better flow of the electrolytic solution to keep a good flow of the electrolyte flowing across the sample. To prepare the apparatus to run, the retaining plate had to be removed, and the sample inserted. Before the retaining plate was put back into place, a back contact of copper wire was inserted between the sample and the plate. Then the plate was tightened to create a seal, which was tested using water. If a good seal was created and no leaks appeared, the system was ready for the acid and anodization. After the anodization run, the electrolytic solution would have to be emptied and rinsed before the sample could be removed.

Figure 3.1 shows the voltage time characteristics for the anodization of an aluminum thin film deposited on a 3" p-type silicon wafer. The aluminum layer was 75nm thick and was thermally evaporated. The current density for the anodization was 10 mA/cm^2. The voltage time curve indicates the formation of a porous alumina layer. The voltage rises as a non-porous alumina layer is formed, then drops as the pores are formed and widened, after which a semi-steady state voltage is reached as the pores propagate. The rise and levelness at the end is believed to be caused by an interaction of the electrolytic solution and the barrier layer. After the chemical reaches the silicon substrate it causes an open circuit, as indicated by the rapid rise in voltage.

While the voltage time characteristics suggested the formation of porous alumina, it was found in visual inspection that there was nothing left on the silicon wafer after the anoidzation. This was one of the earlier attempts by the Nanostructures Research Group in the anodization of

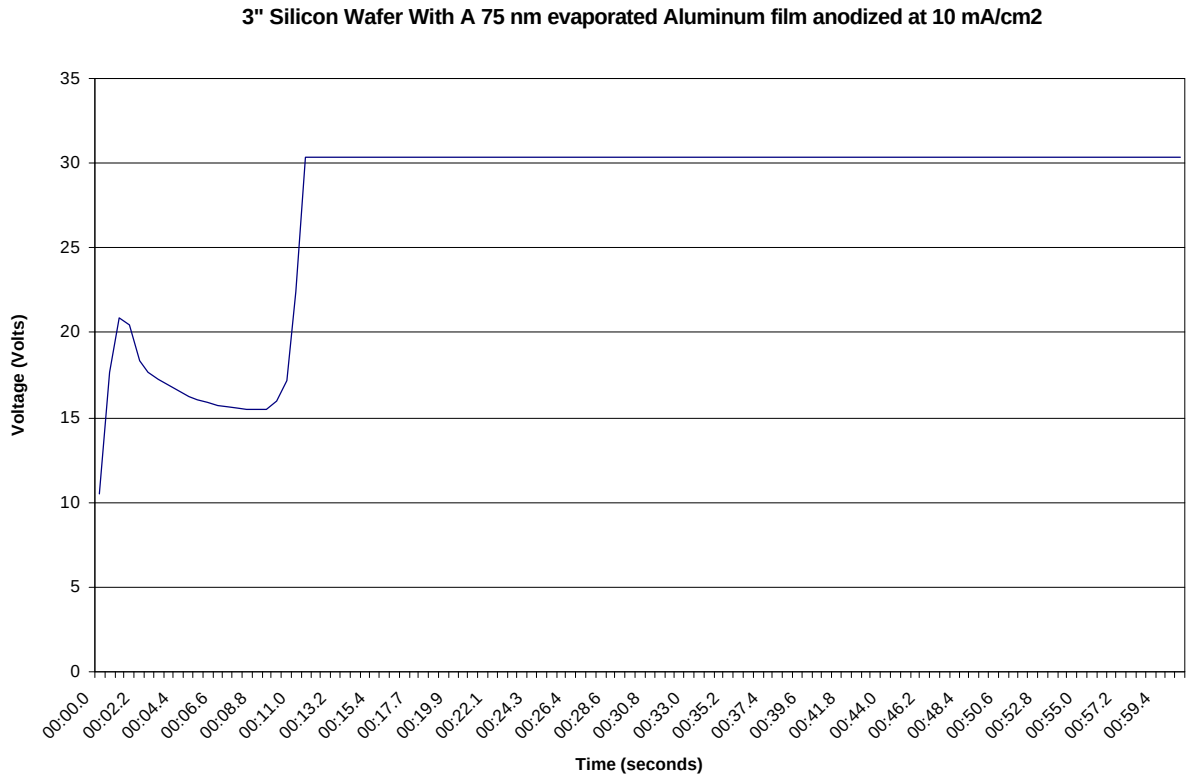

Figure 3.1 Voltage Time characteristic curve for the anodization of a 3" - 75 nm evaporated Aluminum film

thin films. It was feared that the anodization was allowed to run for too long. This was confirmed when the anodization was ran for only two minutes. After the voltage saturated, the layer of alumina was visibly observed to be present.

This apparatus had many disadvantages. First, the sample size was limited to 2 ½" diameter. Second, this apparatus was time consuming; for each run the electrolyte was needed to be transferred in and out at the beginning and end of anodization. Leak testing with water involved similar steps thus adding to the process time. It was also decided that 3" wafers were not economically efficient for process development This setup, however, demonstrated the feasibility of large area anodization. In order to overcome these problems and for the ability to anodize smaller size wafers, an automated apparatus was designed and built [35]. This apparatus was

designed to limit acid handling. All motion, lateral and vertical, was controlled from a controller box outside the acid hood. The sample was then held to a block of Teflon against a point contact to the back contact plate using an air vacuum hand pump. Once the sample was secured, the center block was lowered until the sample was submerged in the electrolytic solution. Once submerged, the anodization process was carried out. After the completion of anodization, the center block was raised and allowed to drain off the acid. The block was then moved over to a rinse dish and lowered into it. After rinsing, the air vacuum was released and the sample removed.

The purpose of the automated apparatus was to decrease the amount of time to run an anodization and to allow smaller samples to be run. It achieved both objectives. The time it took to run an anodization was cut by over a third of the time compared to the large area apparatus. Also with the air vacuum hand pump system to hold the wafers, any size of sample could be used.

Figure 3.2 shows a typical voltage time characteristic curve for this apparatus. It has the general trend of what was seen with the large area anodization apparatus and of bulk Aluminum. However, a problem started to show up with this apparatus. It was noticed that the aluminum was not evenly anodized across the wafer. This was true even for very small samples. It was also observed that the aluminum contact on the back of the wafer was getting etched away, which was not expected. It was postulated that the anodization current was flowing through the edge of the wafer, thus etching the back aluminum layer. This gave rise to an uneven current distribution to the sample, thus causing uneven anodization rates across the wafer.

In order to solve this problem, an improved apparatus was designed and built[36]. Special attention was given to keep the back contact away from the electrolytic solution. Also a solid piece of copper was used for the back contact instead of the point contact in the automated apparatus. The cover for the apparatus had a ½" diameter hole, with an attached ½" O-ring and openings for studs to slide in and tighten down. An O-ring was inserted around the copper plate contact on the base of the apparatus so when the top was tightened down onto the base with four

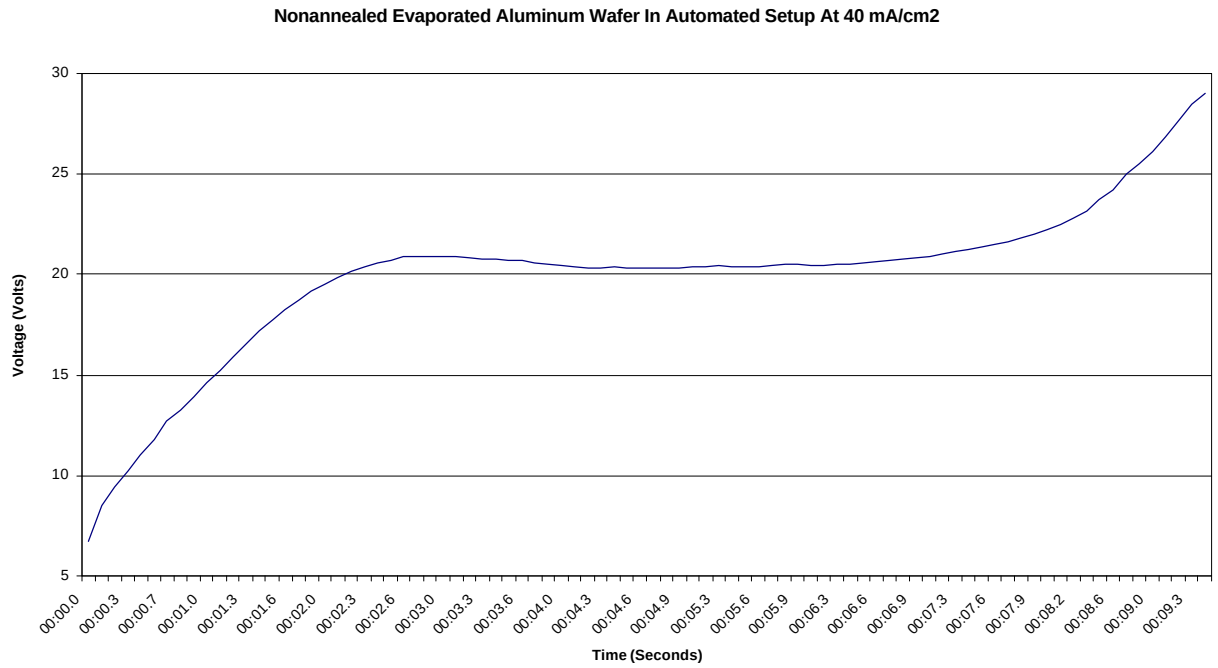

Figure 3.2 Typical Voltage Time characteristic for automated apparatus

teflon nuts, a good seal was formed on the wafer around the area to be anodized. After the sample was seated, the apparatus was immersed into the electrolytic solution. The instrument hookups were then connected and then the sample was anodized. After the anodization, the connections were taken off and the apparatus removed from the solution and rinsed. Finally the top was removed and the sample removed, rinsed and dried. Figure 3.3 schematically shows this apparatus [44].

Figure 3.4 shows a typical voltage time characteristics obtained in the new apparatus. The characteristic curve is similar to what is expected and the samples were observed to be visually uniform across the wafer. This apparatus was used for all anodizations performed in this research. Besides providing the ability to uniformly anodize different size wafers, this apparatus significantly improved wafer throughput and process safety.

Teflon Apparatus

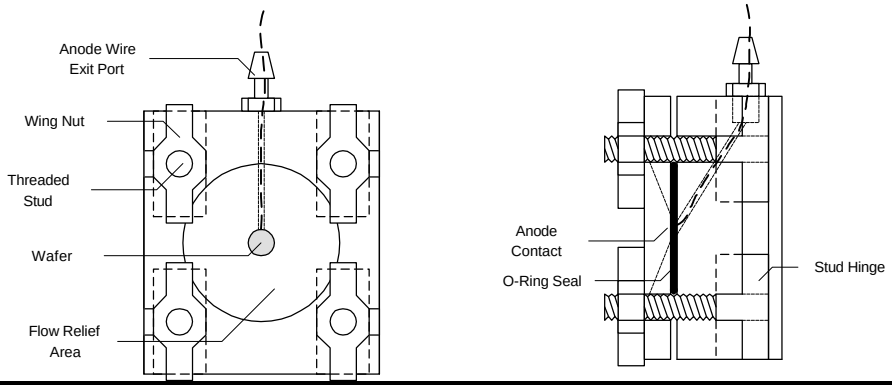

Figure 3.3 Schematic of teflon apparatus

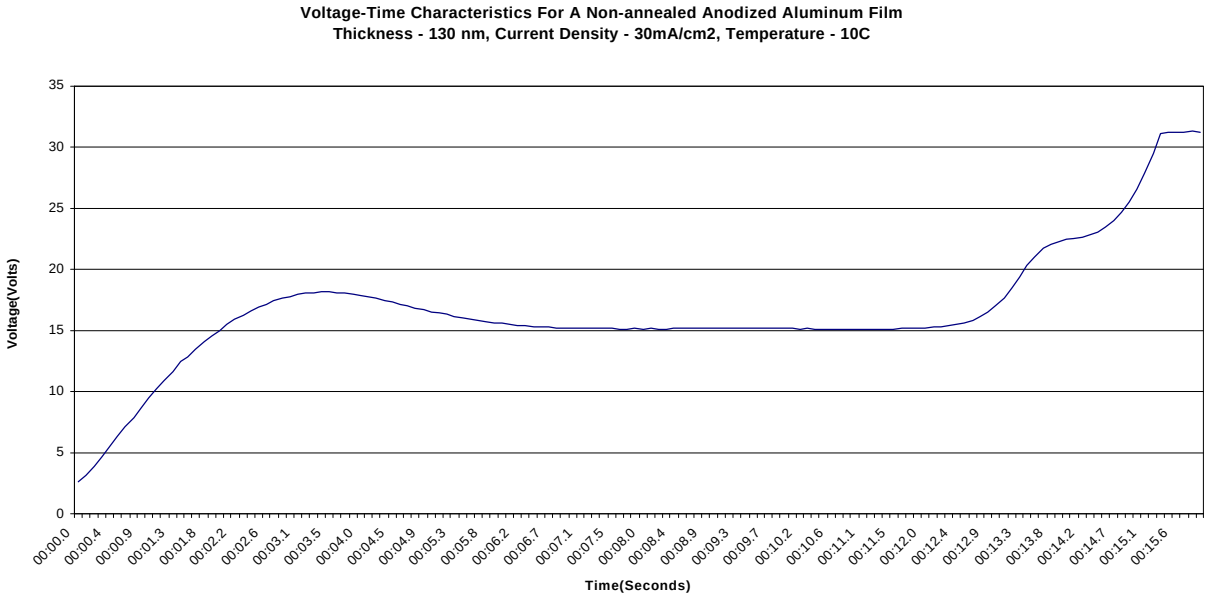

Figure 3.4 Typical voltage time curve for anodization in the teflon apparatus

4. Process Development for Thin Film Templates

4.1 Fabrication Procedure

4.1.1 Cleaning Process

The first step in this fabrication process was to clean the silicon wafers that were being used. This process was done using the Summa clean technique because it removed any metal from the wafer. The process starts with heating Summa clean to 60°C. The wafers were next inserted in to the heated Summa clean. They were removed 30 minutes later, and rinsed in DI water for 10 minutes. As the wafers are rinsing, a 100:1 HF solution was made. The HF dip is used to strip off the native oxide on the wafer. After the wafers are rinsed, they are dipped in the HF solution for 3 minutes. Once again the wafers are rinsed for 10 minutes to remove any remaining acid and dried with Nitrogen.

4.1.2 Aluminum Film Deposition

In order to run any anodization processes, the first step was to have samples that were coated with a metal. Two methods of deposition were investigated. The first was evaporation of 99.99% pure Al, and the second was sputtering of 99.99%Aluminum-1%Copper and 99.999% Aluminum.

In order to achieve the evaporation of Aluminum, the evaporation station had to be rewired and brought back up to running condition. After in running state, several techniques were tried. The first technique was setting the sample a couple of inches away from the source target. This had to be done because the planetary rotation system was not yet in a working state. To run an evaporation, the pressure was taken down to 5.6×10^{-6} Torr, and the source shutter was open for a determined amount of time to get the thickness desired.

After the planetary rotation was brought to running status, the samples were attached to the planetaries. The planetary motion would be turned on and the source shutter open. The time for deposition was different than for the sample a couple of inches from the target, so a new deposition rate had to be calibrated.

These samples were then anodized and Figure 4.1 shows a typical curve for the anodization. The curve is similar to the bulk curves, but instead of holding at constant voltage during pore propagation, the voltage starts to rise. This rise is attributed to the unevenness of the thermally evaporated aluminum film. So, as the pores start hitting the Silicon substrate the voltage starts to rise. Also noted on the thermal evaporated aluminum films an adhesion problem of the aluminum to Silicon. When the anodized samples were inspected visually, it was observed that the alumina was peeling off.. This was attributed to other impurity materials in the evaporator chamber mixing in with the Aluminum. An e-beam evaporated aluminum film was deposited at Notre Dame. When this sample was anodized, the voltage increase was not detected, and the

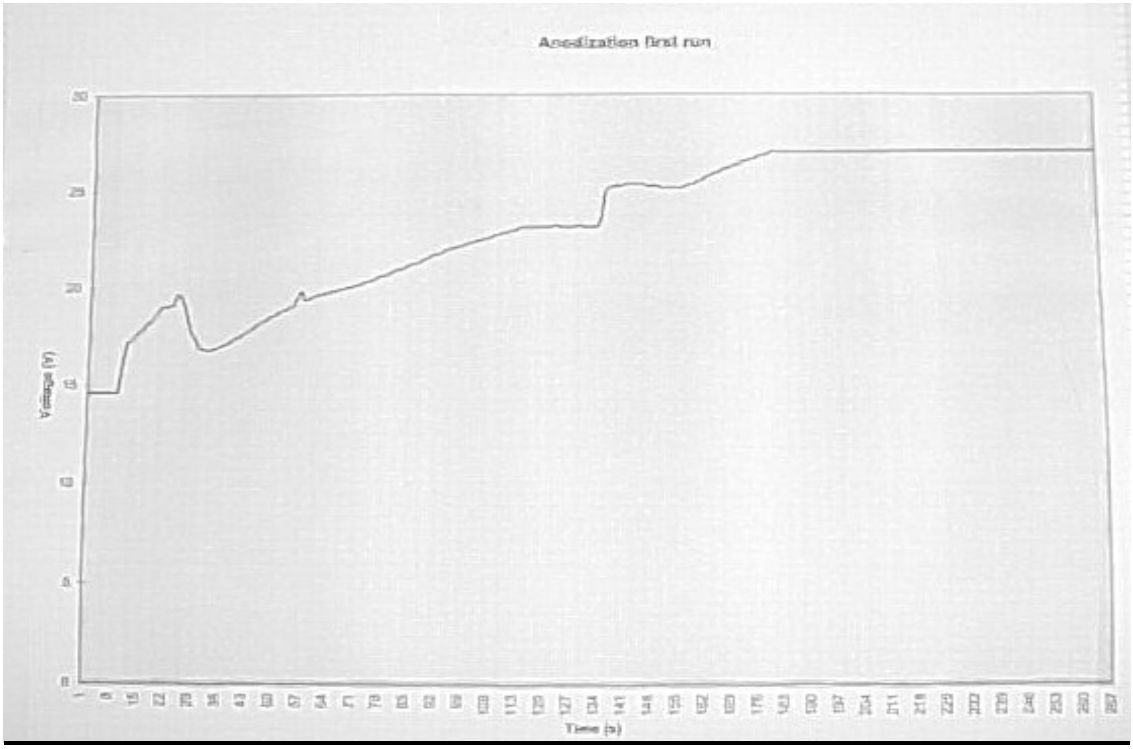

Figure 4.1 Typical voltage time characteristics for an evaporated film

alumina remained intact on the silicon. So it is possible to put down an even evaporated layer of aluminum and anodize it.

Since thermal evaporation of thin aluminum films was problematic, a different method was tried. The second method of deposition was magnetron sputtering. This method deposited an Aluminum-Copper alloy onto the samples. Most of the samples run in this research were deposited using sputtering deposition of Aluminum.

Figure 4.2 shows a typical voltage time characteristic for a sputtered aluminum thin film on a silicon wafer that not annealed. It was noticed that the voltage did not increase steadily after it was thought to hit the silicon substrate. Instead of increasing steadily, the voltage seemed to level off half way up the rise and then it held steady for a few seconds before continuing its rise. The hypothesis for this is that when the barrier layer starts decreasing in size, the voltage starts to rise. After the barrier layer anodizes so far, a new anodization pattern occurs. If imaging was possible, several tests could be run to see what kind of reaction is taking place. At this time this is only a hypothesis.

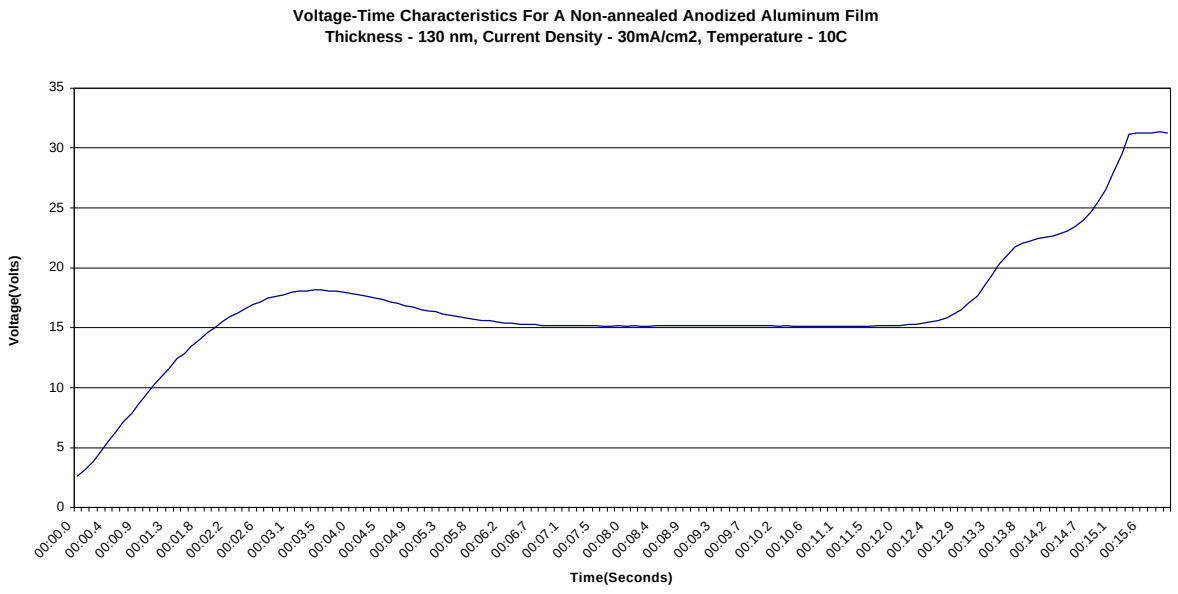

Figure 4.2 Typical voltage time curve for a nonannealed thin film

To increase adhesion and improve the ohmic back contact, the aluminum deposited on the back of the wafer was annealed in a 450°C N_2 oven for thirty minutes. After annealing, the front layer was deposited and annealed at 400°C for 30 minutes. However, annealing of the front aluminum layer produced an interesting effect as seen in Figure 4.3. A feature is observed in the voltage time characteristic as the anodization hits the silicon surface. It was determined that the magnitude of this feature is dependent on the anneal time. Figure 4.4 show a voltage time curve for a 120 minute anneal of the front aluminum layer.

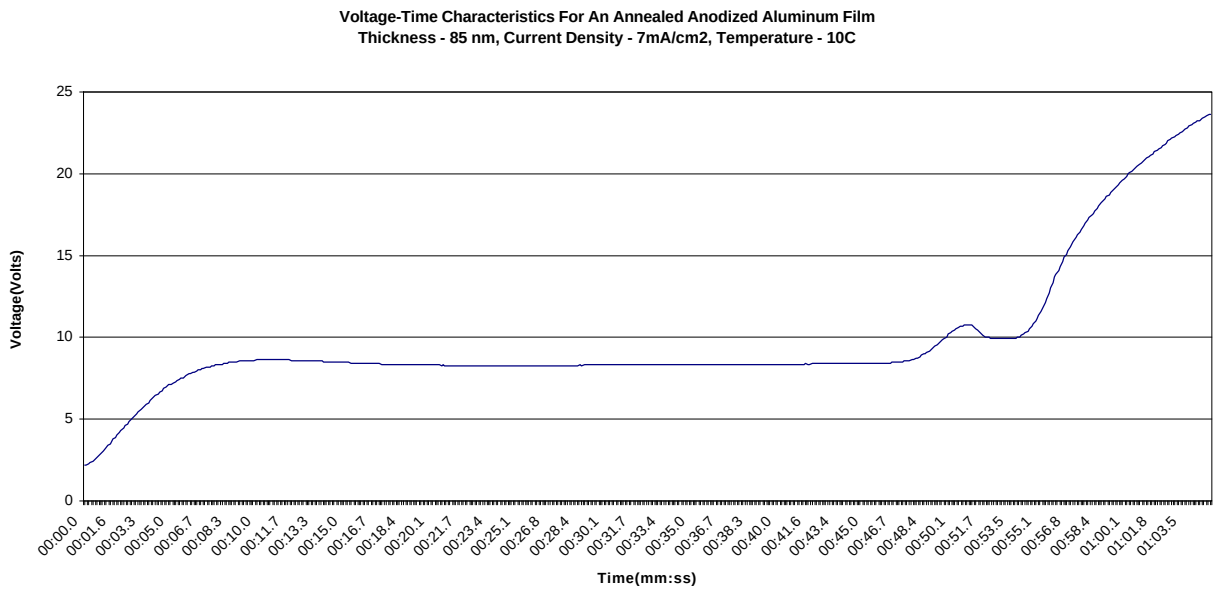

Figure 4.3 Voltage Time curve for an annealed aluminum thin film

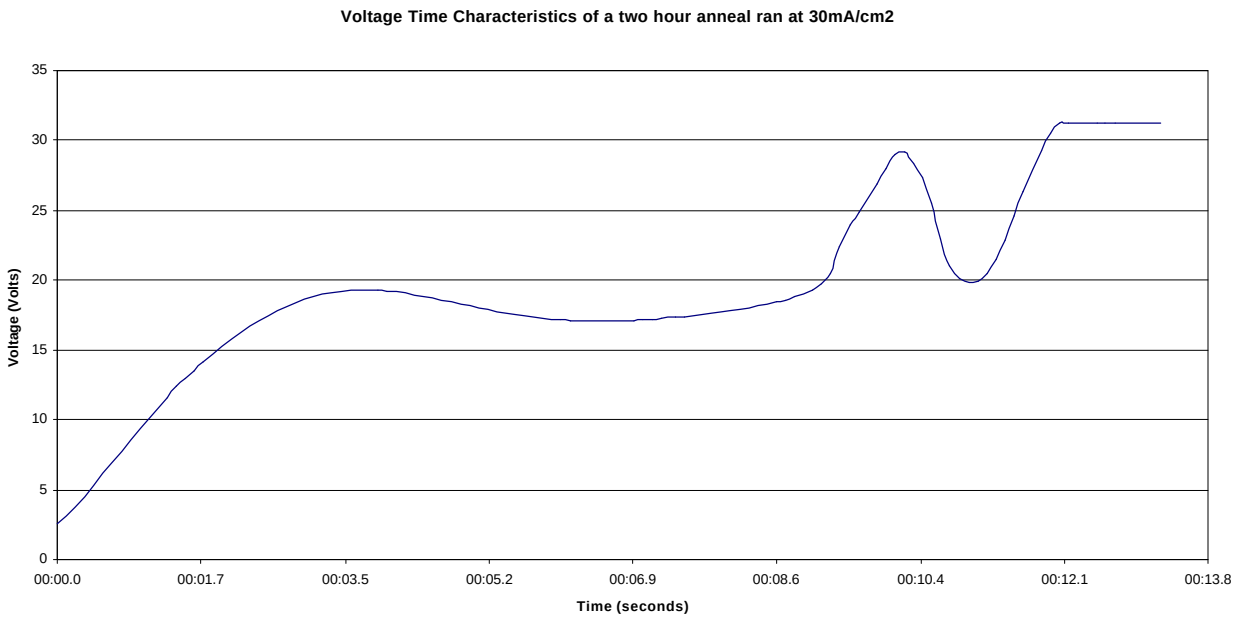

Figure 4.4 Voltage Time characteristic for a 2 hour annealed sample

Initial imaging was performed using an Atomic Force Microscope. Figure 4.5 shows an Atomic Force Microscope(AFM) image of one sample. As can be seen in the figure, the grain boundaries are easy to identify. The small pieces around the grain boundaries are believed to be the pores. A Field Emission Scanning Electron Microscope (FESEM) image is shown in Figure 4.6 for comparison. The pore non uniformity is believed to be due to the aluminum layer not being pure aluminum but instead an aluminum copper mix.

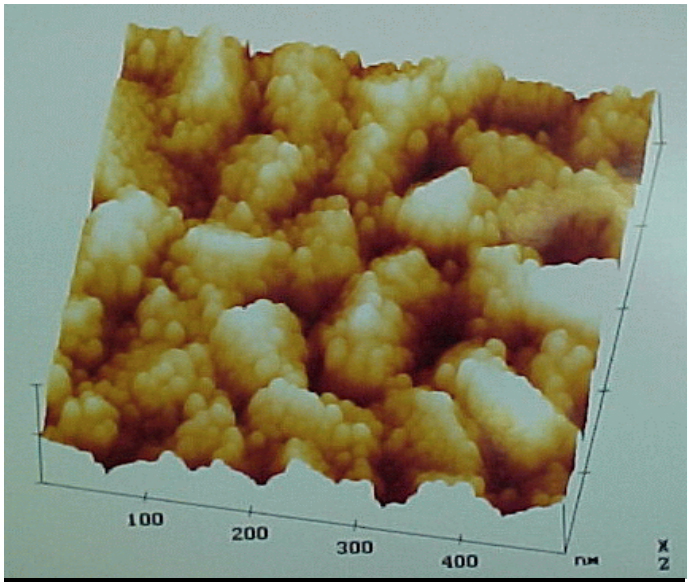

Figure 4.5 AFM image of anodized aluminum thin film

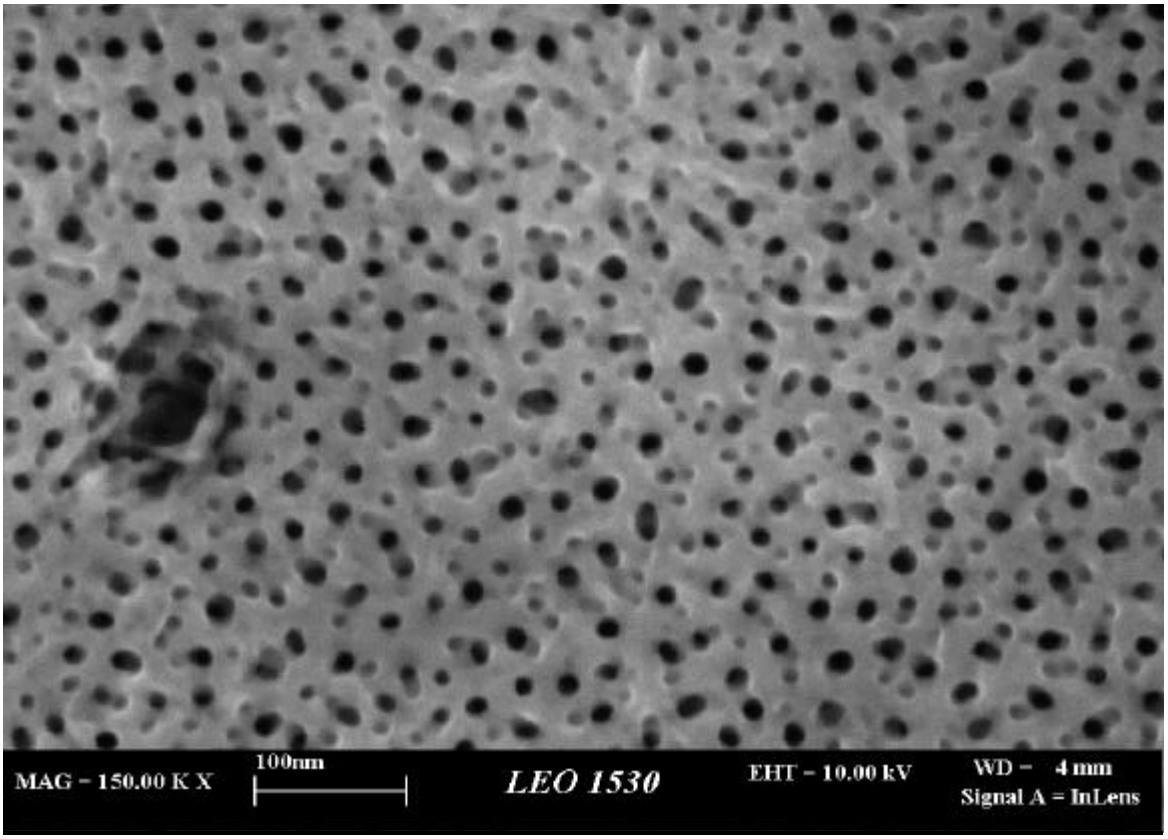

Figure 4.6 FESEM image of an anodized aluminum thin film

4.1.3 Anodization

The next step after thin film annealing is anodization. Figure 4.7 shows the block diagram of the anodization setup. The data acquisition consists of a PC computer and an HP 34401A Multimeter. An HP E3632A DC power supply is used as the power source. To chill our electrolytic solution a Jubalo F-10 chiller is used. To circulate the solution through the chiller a Masterflex peristalsis pump is used. The electrolytic solution is a 20% by volume H_2SO_4 and DI water mixture.

The first step in using this setup was to experimentally determine the flow rate of the peristalsis pump. There are ten settings on the pump and the flow rate ranges from 0 mL/min to 495 mL/min. The chiller was then attached to see what rates would hold the temperature steady.

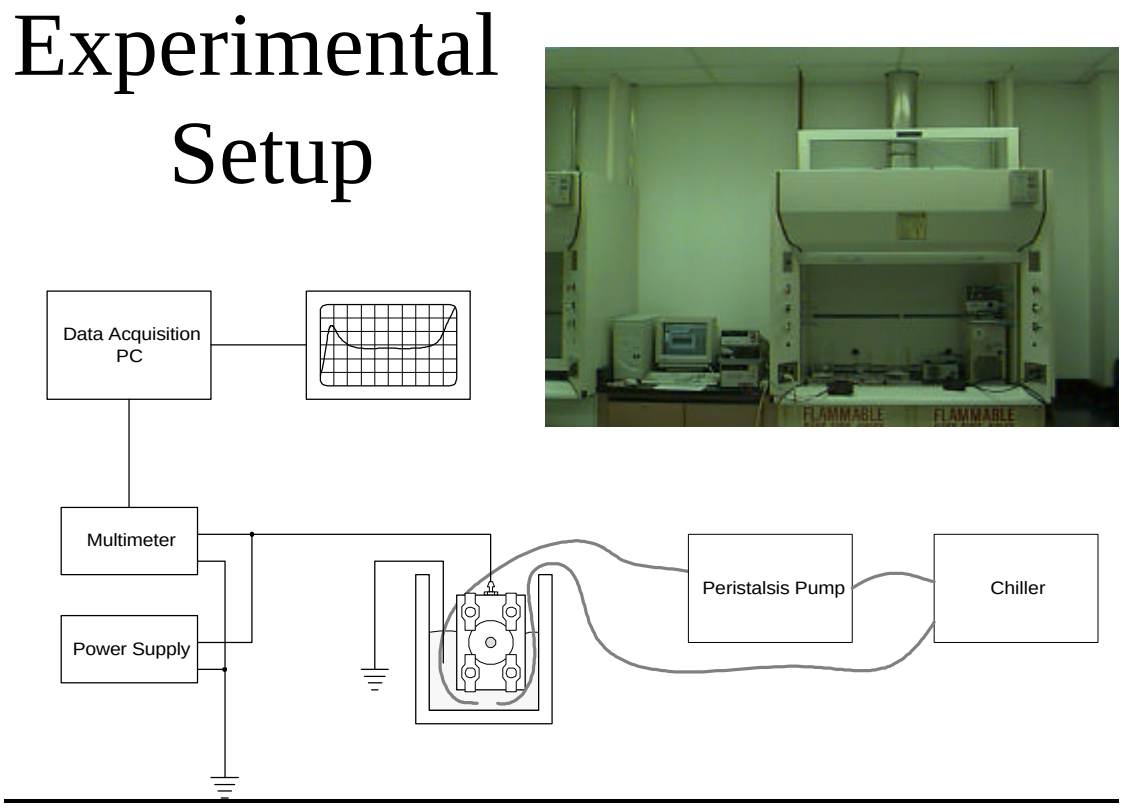

Figure 4.7 Block Diagram of the anodization setup

It was determined that setting 3 on the pump would work well at a rate of 100 mL/min. It was also noted that there is about a 10°C difference between the chiller and the actual temperature of the electrolytic solution. So the chiller is set for -9°C and an electrolytic solution temperature of 1°C to 3°C is obtained. After the temperature is stabilized, anodization is carried out by sending a constant current between the substrate and the electrolyte.

4.1.4 Pore Widening

After anodization, the pores are widened in phosphoric acid to remove the initial non uniform alumina layer. Crouse determined that after 8 minutes in phosphoric acid the barrier layer is undercut and lifts off from the substrate [45]. Garman used CV characterization to see if pore widening had any affect on template properties. He showed that pore widening of the samples improved the flat band voltage distribution [44].

Pore widening is performed in 5% phosphoric acid for between 0 to 6 minutes. The samples were then rinsed for 30 minutes in DI water to insure no remnants of the anodization solution were left on them. The samples were then pore widened, and once again rinsed for 30 minutes to remove any phosphoric acid solution. Figure 4.8 shows an FESEM picture of pore widened porous alumina. As can be seen the pores are very uniform in size. This sample was pore widened for 6 minutes and has Nickel deposited in some of the pores via constant current electro deposition.

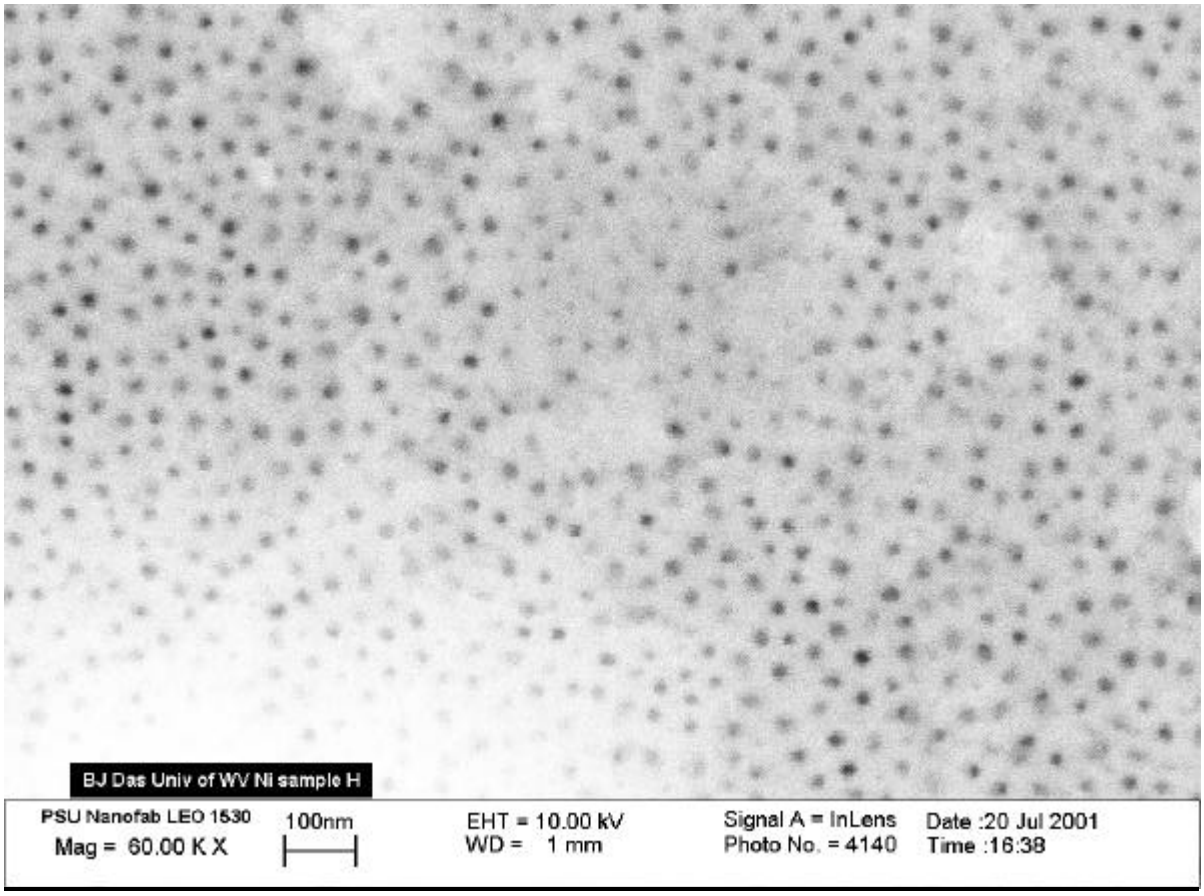

Figure 4.8 FESEM image of anodized aluminum thin film pore widened for 6 minutes with nickel deposited in some of the pores.

4.2 Multilayer Anodization

With the confidence that the anodization technique was successful, the technique was tried on multilayer films. What is meant by multilayer anodization, is that a layer of aluminum is first sputtered onto the silicon wafer and anodize. After rinsing, a second layer of Aluminum is sputtered on top of the alumina template, and is then anodized. Figure 4.9 shows a cross section of what the sample should look like. The first anodization was a typical anodization. Figure 4.10 shows the second layer anodization voltage time curve. It is unclear whether the second anodization made the pores in the same spots as the first anodization, or whether they were

formed at different locations. A cross section needs to be taken to see those results, but Figure 4.10 at least confirms that the anodization process works on more than one level.

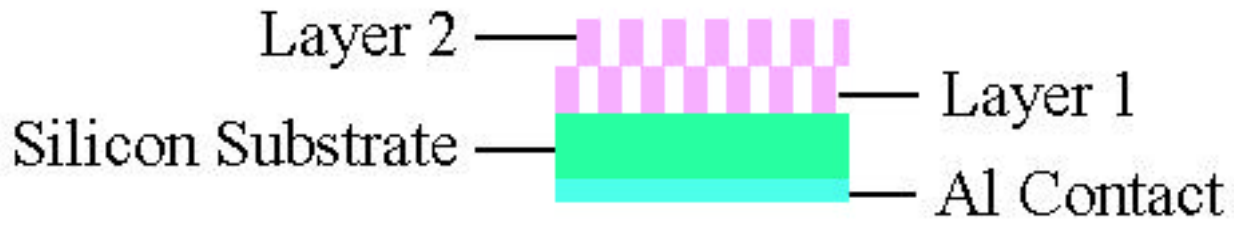

Figure 4.9 Theoretical cross section of a multilayer structure

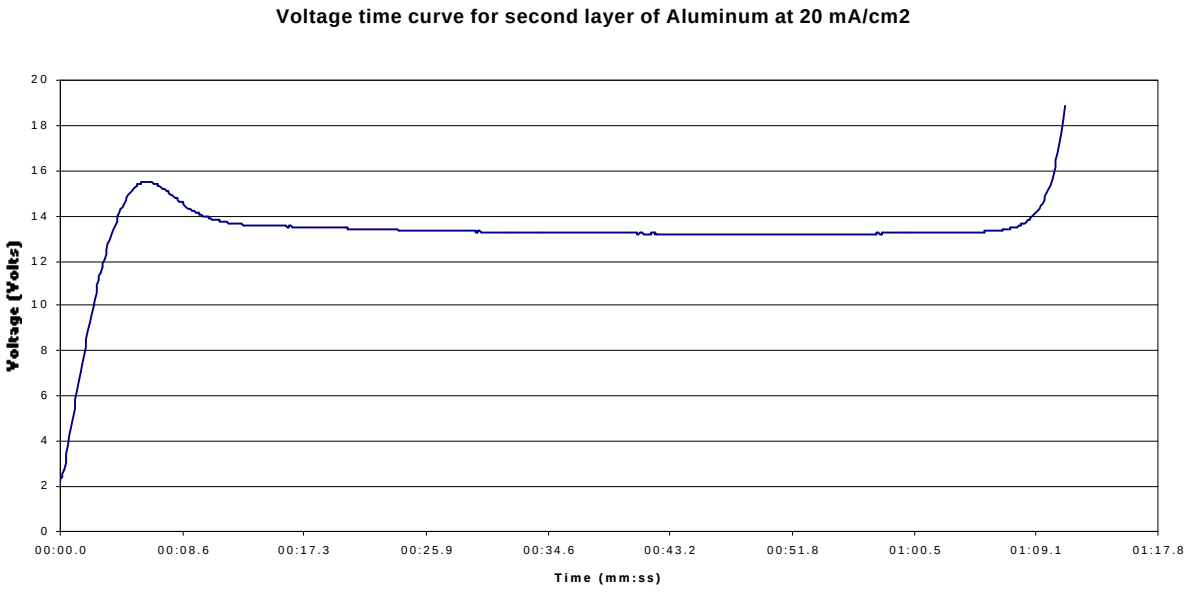

Figure 4.10 Voltage Time curve for second layer anodization

4.3 Other Substrates

4.3.1 ITO and Glass Slides

Besides running anodizations of Aluminum deposited on silicon substrates, we also tried glass slides and glass slides coated with Indium Tin Oxide (ITO) as substrates. The first problem associated with this was how to make contact with the aluminum and the back contact. With Silicon this was not a problem since a back contact could be made to the substrate. So contacts were made of aluminum foil and wrapped around the glass substrate as shown in Figure 4.11. This made the contacts to the aluminum via the front aluminum layer. The teflon apparatus contact pad was lowered so the glass slide would seal, and the anodization was run. Figure 4.12 shows a voltage time characteristic curve for an aluminum film on a glass slide. When the glass slide was observed, you could see through it, which makes sense since alumina is transparent. Figure 4.13 shows the results of anodization of aluminum on an ITO substrate. As can be seen the voltage time curve starts out normally, but anomalous signals are observed as the anodization begins to hit the ITO layer. This is possibly due to localized degradation of the ITO in sulfuric acid.

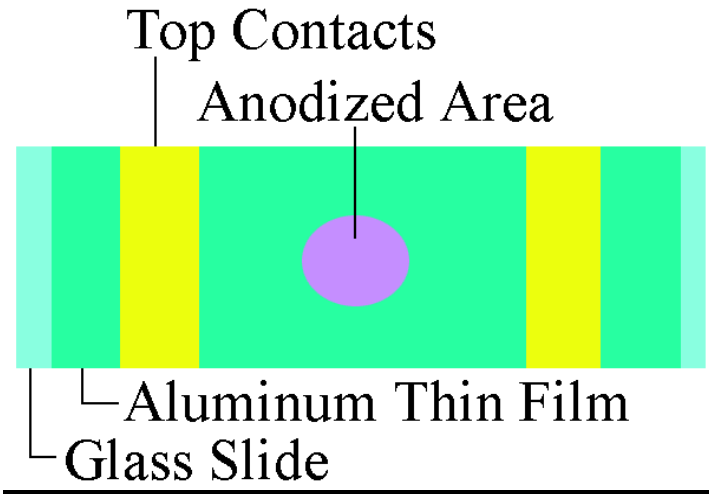

Figure 4.11 Contact setup for glass slide substrates

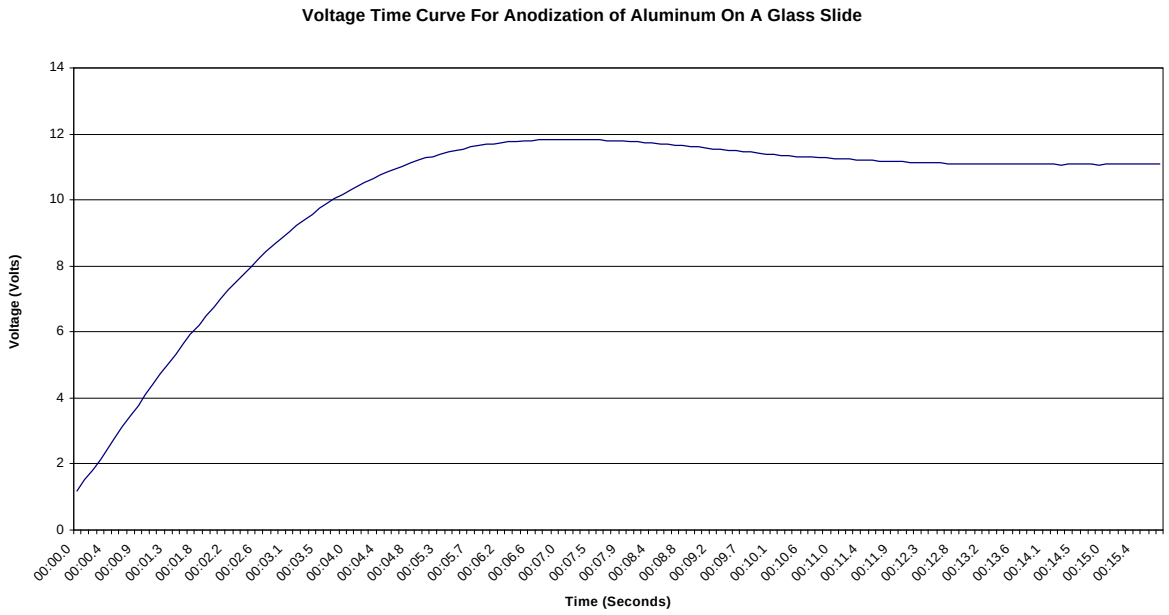

Figure 4.12 Voltage Time Curve for anodization of a glass slide

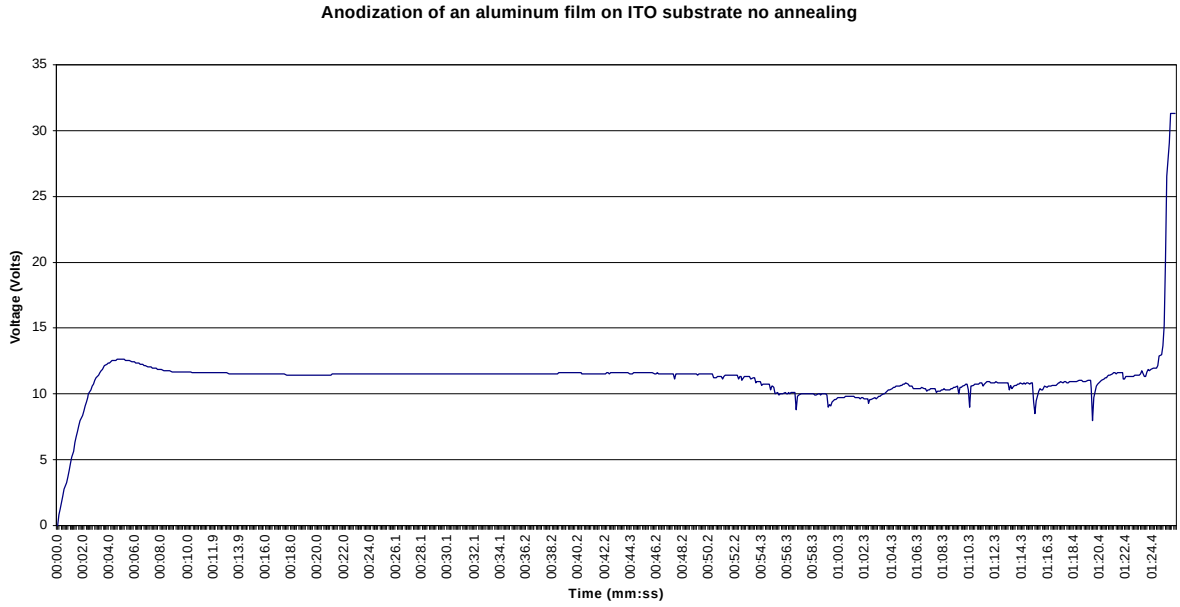

Figure 4.13 Voltage Time curve for anodization of aluminum on an ITO substrate

4.3.2 Platinum Contact Layer

For electo optic devices, a contact layer is needed under the alumina to make contacts to both ends of the nanostructures. Silicon substrates were used initially since they provided a contact to the aluminum layer. However, when semiconductor materials are deposited into the pores, it will be difficult to make a contact with the semiconductor material through the silicon substrate. So a contact layer needs to be added. In some cases ITO can be used as discussed in the previous section, but if one does not have access to ITO covered slides, then another alternative has to be found. In this case a layer of Platinum was deposited on the silicon before the aluminum. Platinum is inert when in contact with sulphuric and phosphoric acid. Figure 4.14 shows the voltage time characteristics of a platinum aluminum layer. The platinum should provide a good contact to the semiconductor material on both p and n type silicon wafers..

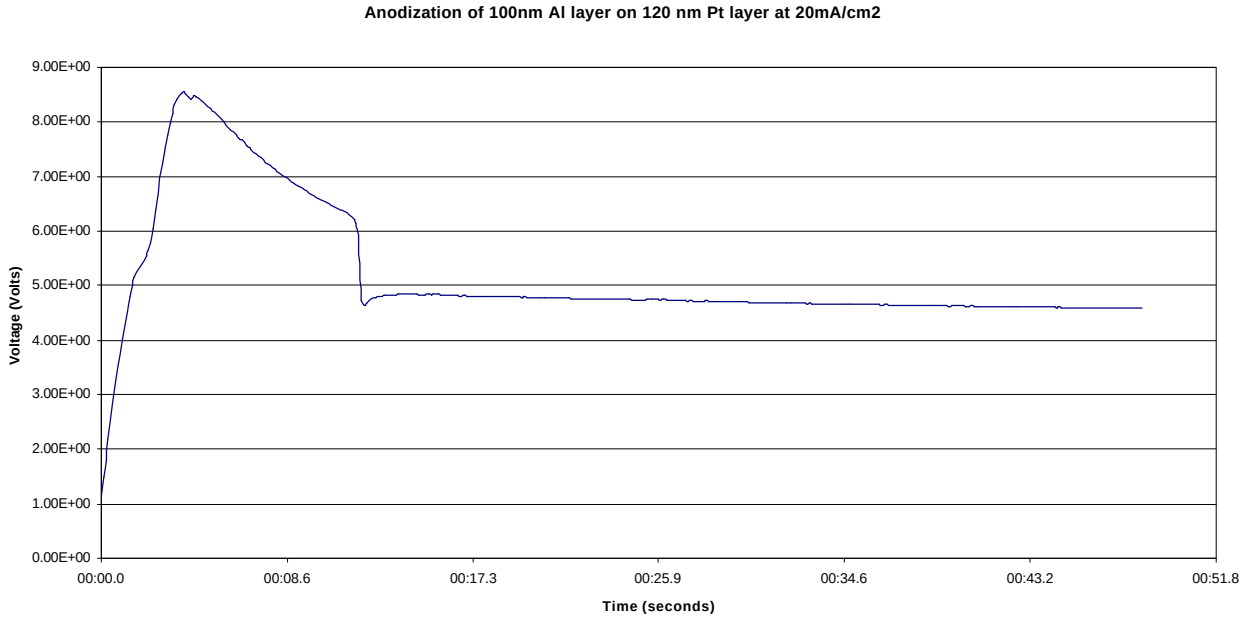

Figure 4.14 Voltage time curve for anodization of aluminum on platinum

4.3.3 Silicon Carbide

Another substrate that was tried was Silicon Carbide wafers. They were prepared the same way as the silicon substrates with aluminum on the front and the back of the wafer. The voltage time characteristics for an anodization is shown in Figure 4.15. These voltage time curves are very similar to those for silicon. Next, a high resistivity silicon carbide layer was tried. The voltage time curve is shown in Figure 4.16. As with the normal silicon carbide wafers, the curves look similar to that of previous anodization runs. It was also noted that the Silicon Carbide samples do not have the dip when the anodization reaches the substrate as occurred with Silicon samples.

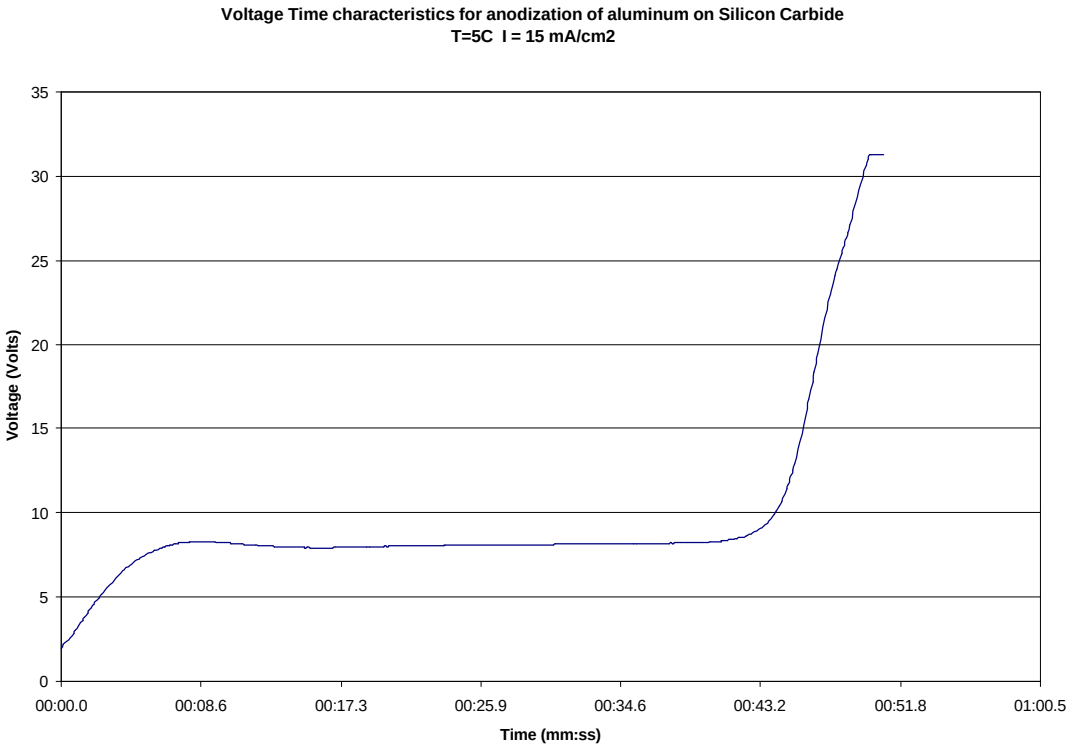

Figure 4.15 Voltage Time curve for Aluminum on Silicon Carbide substrates

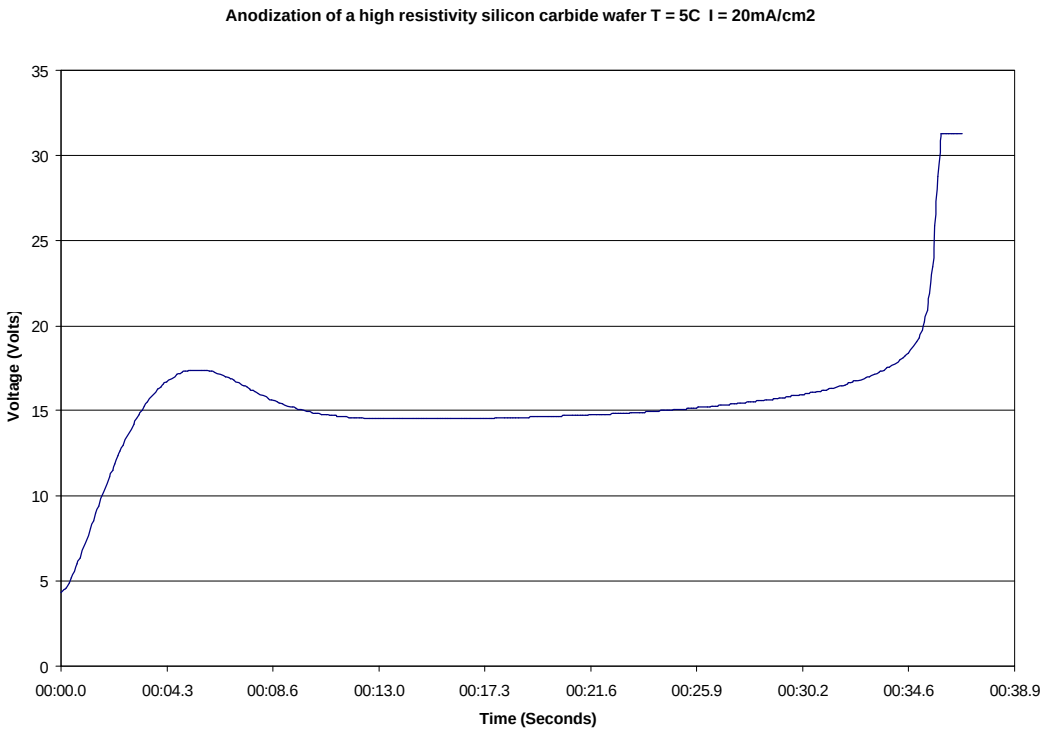

Figure 4.16 Voltage time curve for high resistivity Silicon Carbide substrates

4.4 Anodization Data

From each anodization curve, the following information could be observed; barrier formation, pore formation, and anodization rate. Before looking at the data, an understanding of how the data was calculated is needed. Figure 4.17 shows a voltage time curve with the various regions on it. To calculate the barrier formation rate, the time it takes to reach the first peak was determined. To calculate the pore formation rate, the time it took for the barrier layer to form was subtracted from the time where pore propagation began. And finally to calculate the anodization rate, the time it took for the pores to reach the substrate was used. This was then divided by the thickness of the film.

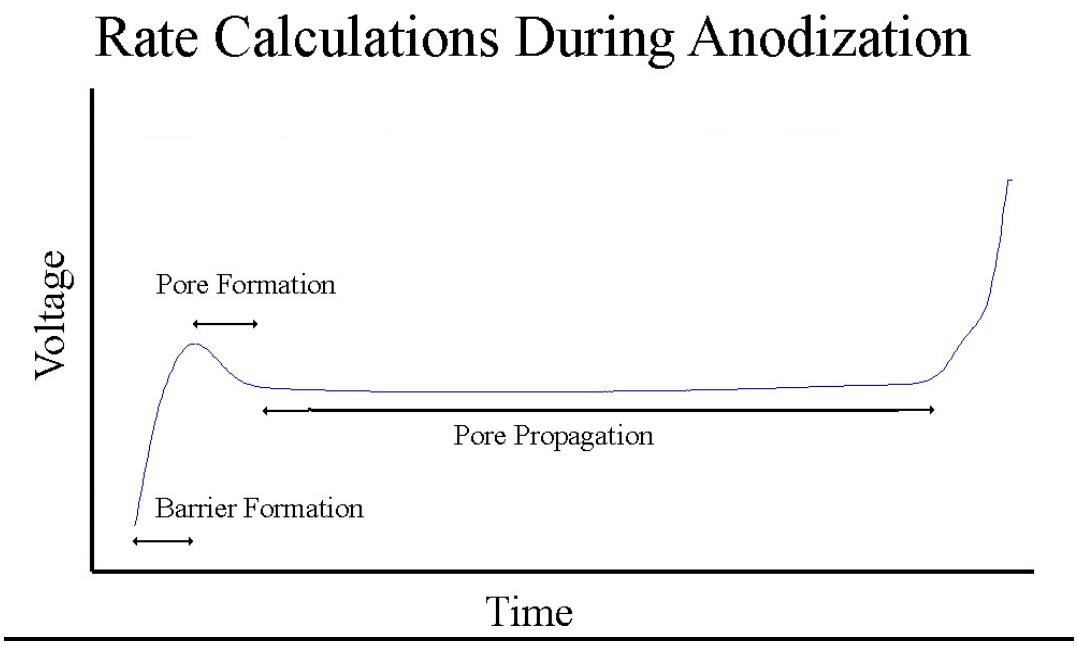

Figure 4.17 How the rates were calculated

The first parameter looked at was the variation of anodization rate with temperature and thickness. Figure 4.18 shows several different temperatures, aluminum thickness, and properties. As can be seen in this figure, the anodization rates for all of the cases are very similar. After about a current density of 30mA/cm^2, the anodization rates start to vary a little more widely.

For an even closer look at these properties, Figure 4.19 looks at the case of constant film thickness while the temperature is varied. Once again the temperature change does not affect the anodization rate significantly. Figure 4.20 looks at constant temperature with varying film thicknesses. And again there is very little variation in the anodization rates.

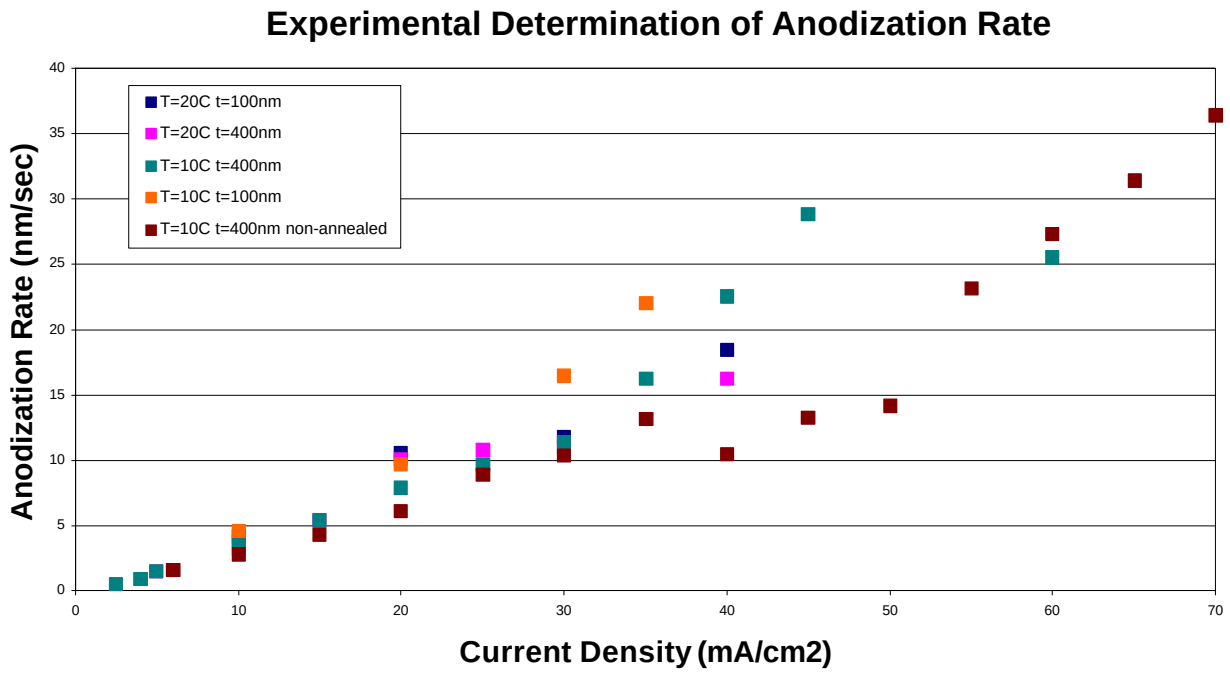

Figure 4.18 Experimental Anodization Rate

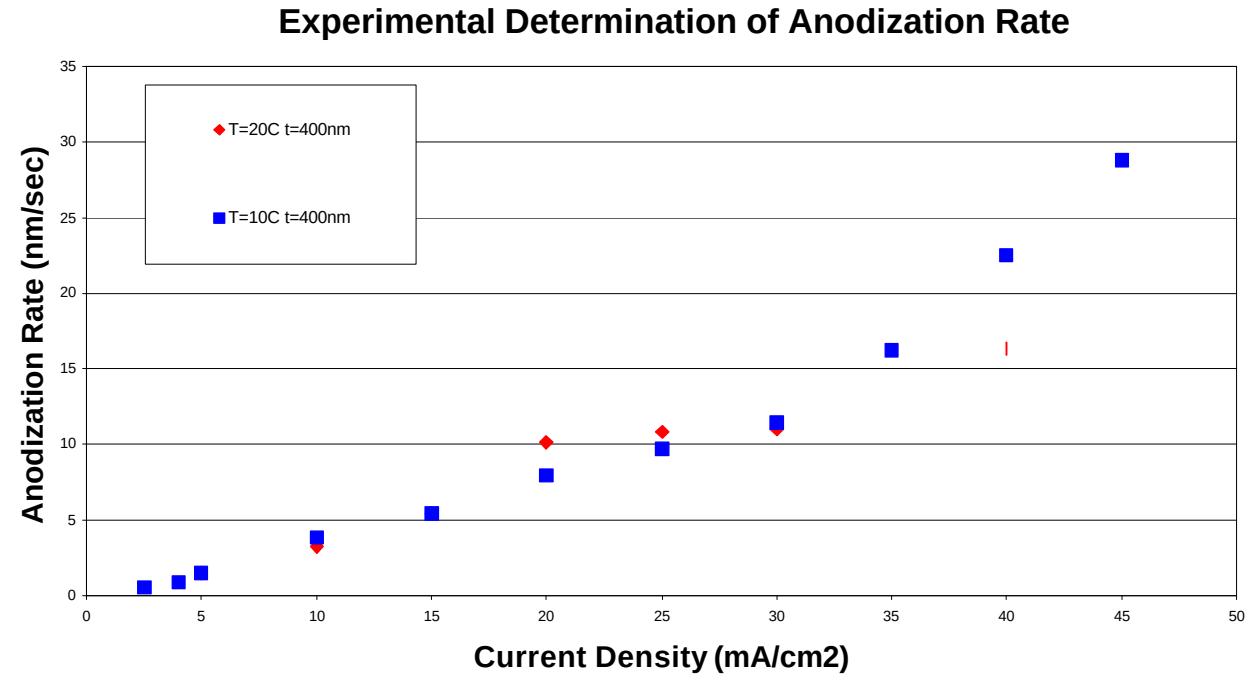

Figure 4.19 Anodization Rate with constant film thickness and varied temperatures

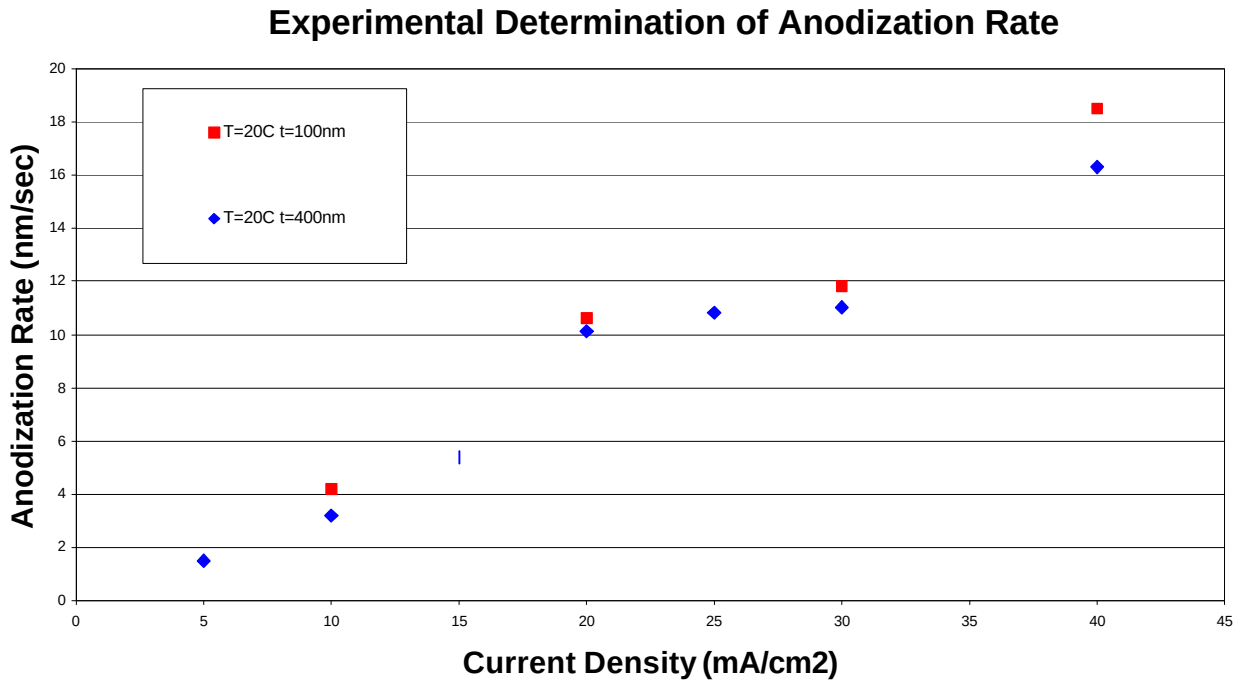

Figure 4.20 Anodizations Rates with constant temperature and varied film thickness

The next parameters looked at were the dependence of barrier layer formation and pore formation on temperature and thickness. Figure 4.21 shows barrier layer formation time as a function of temperature and thickness. As with the anodization rate, the higher the current density the faster the barrier formation is accomplished. The barrier formation is quite consistent even with a change in temperature and a change in thickness. Figure 4.22 looks at stage 2, pore formation, of the anodization process in relation to variances in temperature and thickness. Once again there is not a large change in the time it takes for the pores to form. It is interesting to note that for current densities above 15mA/cm^2 , the pore formation time is about the same.

As mentioned above, an important piece of data that is needed is the pore size and distribution in relation to varying temperatures and thicknesses. Once this data is collected, then most of the necessary data will be recorded for constant current anodizations.

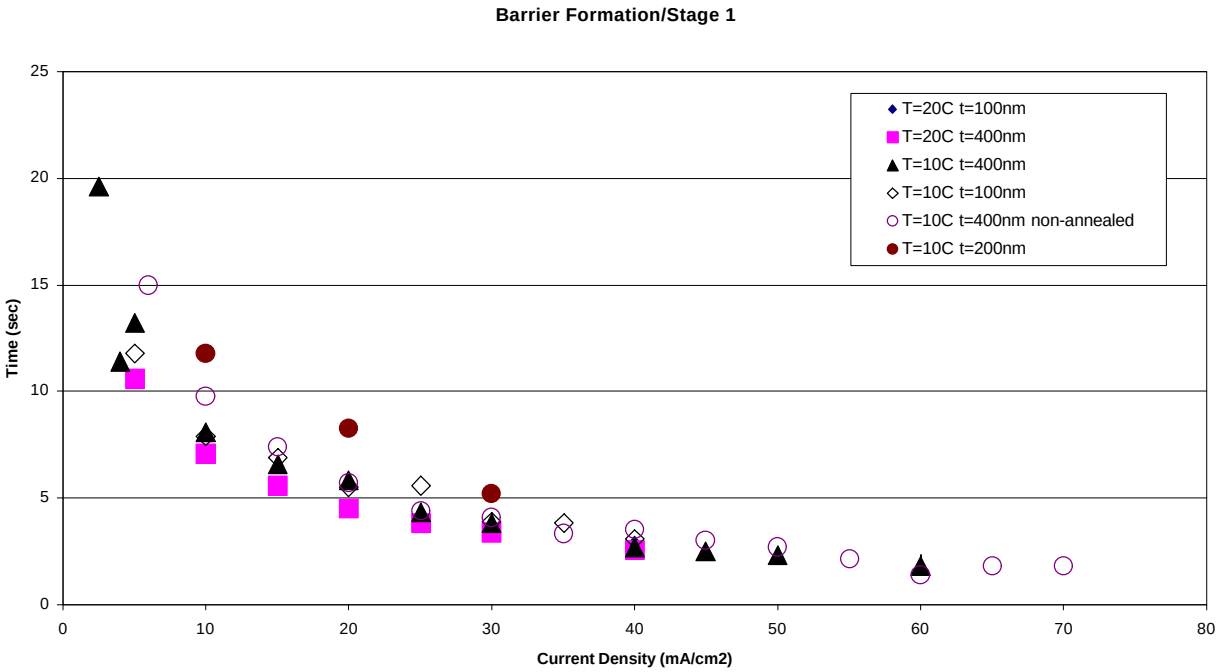

Figure 4.21 Barrier formation rate for anodization

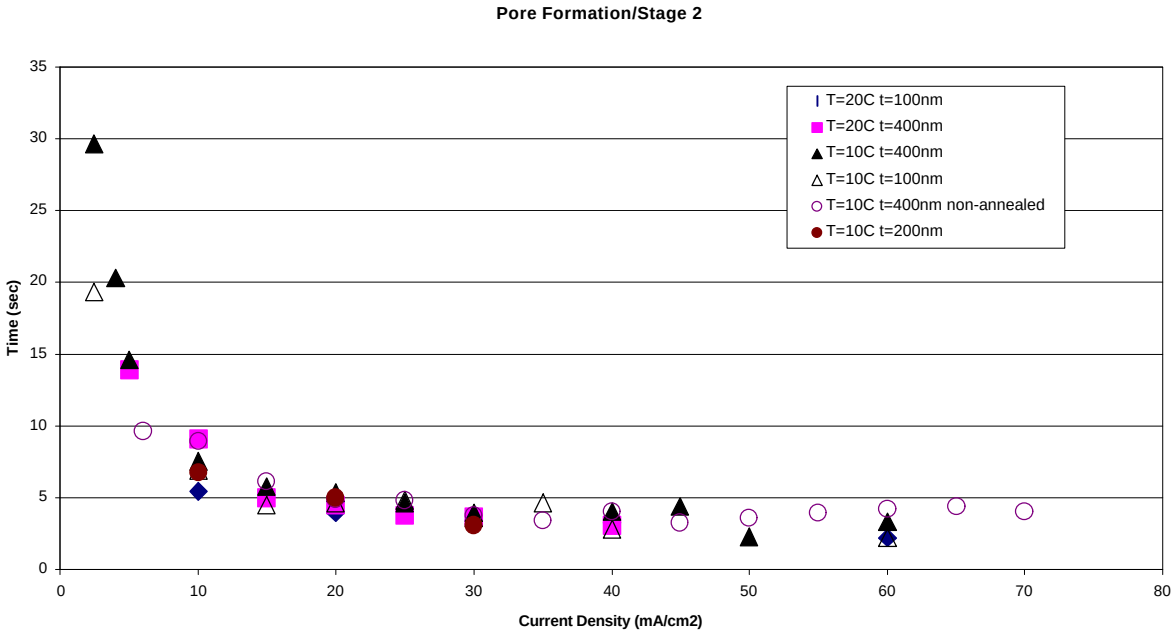

Figure 4.22 Pore formation rate for anodization

5. Conclusions and Future Work

This research has led to a lot more questions to be answered. For instance how does annealing affect the interface between the aluminum and silicon? Why does the voltage at the end of an anodization run changes instead of staying linear? The experiments performed in this research have all been constant current anodization, another avenue to investigate is constant voltage. How much variance are there between the two methods? Does one give more periodic pores than the other? Does the anodization rates change? Another area where experiments are needed is the dependence of pore size distribution on current density. A high powered microscope is needed for this.

The teflon apparatus is still in use today but a few flaws have been noticed. They are minor and can be taken care of easily when time permits. The first is that when the cover is tightened down, there is no set pressure. If a plate was inserted between the studs, then this would not be a problem. Right now, the center of the cover has to be watched to make sure the wing nuts are not tightened down too tight to create a leak. The second problem is the adjustment of height for the sample. Currently three screws are used to adjust the height of the copper back plate. So there is no set height for each substrate type. An easy way for adjustments needs to be designed.

So there is a lot more research that can be done with the proper equipment. I hope to be able to do this research in the near future to complete what I started out to.

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Appendix A

Activity Coefficients

Electrolytes represent a special class of non-ideal mixtures that are different both at the macroscopic level of classical thermodynamics and at the molecular level of statistical thermodynamics [46]. One reason is that electrolytes disassociate differently. Strong electrolytes disassociate completely while weak electrolytes only disassociate to some degree. Knowledge of the mean activity coefficients of mixed aqueous electrolyte solutions in a wide range of concentrations is of fundamental importance for understanding various physiochemical phenomena occurring in hydrometallurgy, electrochemistry, biochemical systems, and other aqueous mixtures of practical and theoretical interest[47].

The rest of this section will look at the different models used to calculate the activity coefficients. The models looked at will include the electromotive force method using the Nernst equation, or better known as the Harned equations, the Debye-Hückel model, Pitzer Ion Interaction Model, and Meissner Corresponding States Model. After looking at each of these models, a comparison of the models will be looked at. These models are only some of the models used to calculate various activity coefficients and not all of the models.

Harned Cell

The electromotive force method, Harned equations, has been demonstrated to be precise for determining mean activity coefficients[48, 49]. Harned created a cell known as the Harned cell that does not have a liquid junction. He then measured the emf for different ionic strengths. This data was then inserted into the Nernst equation to calculate the mean activity coefficient of different electrolyte solutions. Where E is the electromotive force, E^0 is the standard potential of the electrodes used to measure the emf, R is the gas constant, T is the Temperature, F is Faradays Constant, and γ is the activity coefficient of the electrolyte solution.

$$E = E^0 - \frac{RT}{F}\ln g_A g_B$$

Debye-Hückel Model

The theory proposed in 1923 by Debye and Hückel provides a rigorous anchor point for most engineering models of electrolyte solutions[46]. They modeled a dilute electrolyte solution as a mixture of spherical ions of charges immersed in a solvent of constant dielectric strength. This produced the Debye-Hückel limiting law.

$$\log_{10} g_{\pm} = \frac{z_+ z_-}{8p}\left(\frac{F^2}{e_0 D_s RT}\right)^{3/2}\left(\frac{(2000)^{1/2} r_s^{1/2} I^{1/2}}{2.303 N_A}\right)$$

Where γ is the activity coefficient of the electrolyte solution, z_+z_- is the ion charge product, R is the gas constant, T is the Temperature, F is Faraday's Constant, ϵ_0 is permittivity of free space, ρ_s is the density of the solvent, D_s is the dielectric constant, I is the ionic strength, and N_A is Avogadro's number.

Pitzer Model

Pitzer looked at the osmotic pressure of the solution to develop his model. His model is straightforward but mathematically tedious. The Pitzer Ion Interaction Model is given by:

$$\ln g_{\pm} = \left|z_+ z_-\right| f^g + m\left(\frac{2\nu_+\nu_-}{\nu}\right)B_{\pm}^g + m^2\left(\frac{2\left(\nu_+\nu_-\right)^{3/2}}{\nu}\right)C_{\pm}^g$$

$$f^g = -3A_j\left[\frac{I^{1/2}}{1+bI^{1/2}} + \frac{2}{b}\ln\left(1+bI^{1/2}\right)\right]$$

$$B_{\pm}^g = 2b_o + \frac{2b_1}{a^2 I}\left[1-(1+aI^{1/2}-.5a^2 I)\exp(-aI^{1/2})\right]$$

$$A_f = \frac{1}{3}\left(2p(1000)N_A r_s\right)^{1/2}\left(\frac{e^2}{4pe_o D_s kT}\right)^{3/2}$$

The parameters β_0, β_1,$C_{\pm}^{\phi}$ are fitted for each electrolyte and can be looked up. Pitzer recommends setting α = 2.0 and b = 1.2, both in units of (kg/mol)^{½}. Pitzer related his model to the Debye-Hückel model by using the Debye-Hückel term f^{γ}. All other terms are defined the same as in the Debye-Hückel model above.

Meissner Corresponding States Model

Meissner added a couple new parameters to the Debye--Hückel limiting law. This became known as the Meissner model:

$$\Gamma_{ij}^{0} = \left[1 + B(1+.1I)^{q_{ij}^0} - B\right]\Gamma_{ij}^{DH}$$

$$\log_{10}\Gamma_{ij}^{DH} = \frac{-.5107I^{1/2}}{1+CI^{1/2}}$$

$$B = .75 - .065q_{ij}^{0}$$

$$C = 1 + .055q_{ij}^{0}\exp(-.023I^{3})$$

$$C_{\pm}^{g} = \frac{3}{2}C_{\pm}^{f}$$

The above equations are for aqueous electrolytes at 25°C. This model is extremely valuable for multicomponent systems. The q_{ij}^{o} term can be obtained from a lookup table.

As can be seen there are a lot of ways to calculate the mean activity coefficient of electrolyte solutions. The models selected for this paper are representative but by no means inclusive of all the approaches for predicting the activity coefficients of the electrolyte solutions.

The model that is chosen depends on how close to the experimental data one would like to get. The closer one wants the more controllable parameters required in your model. Most of these models are for a single electrolyte compound. Research is still ongoing to better determine this activity coefficient as well as multiple combinations of electrolyte solutions.

Figure A.1, [46] shows an example of several of the models discussed in this paper, along with a couple of other models not discussed. As can be seen in the graph, for lower ionic strengths, most of the models are right on with the experimental data except for the two involving the Debye-Hückel model. As the ionic strength increases, the Pitzer model still closely agrees with the experimental data, but the Meissner and Chen models start to separate. This is not true for all electrolyte solutions, sometimes all of the models vary form the experimental, and other times the Pitzer model disagrees but the Meisnner and or Chen models could agree. So as research continues in this area, researchers will use what models they currently have to predict the activity coefficients of electrolyte systems.

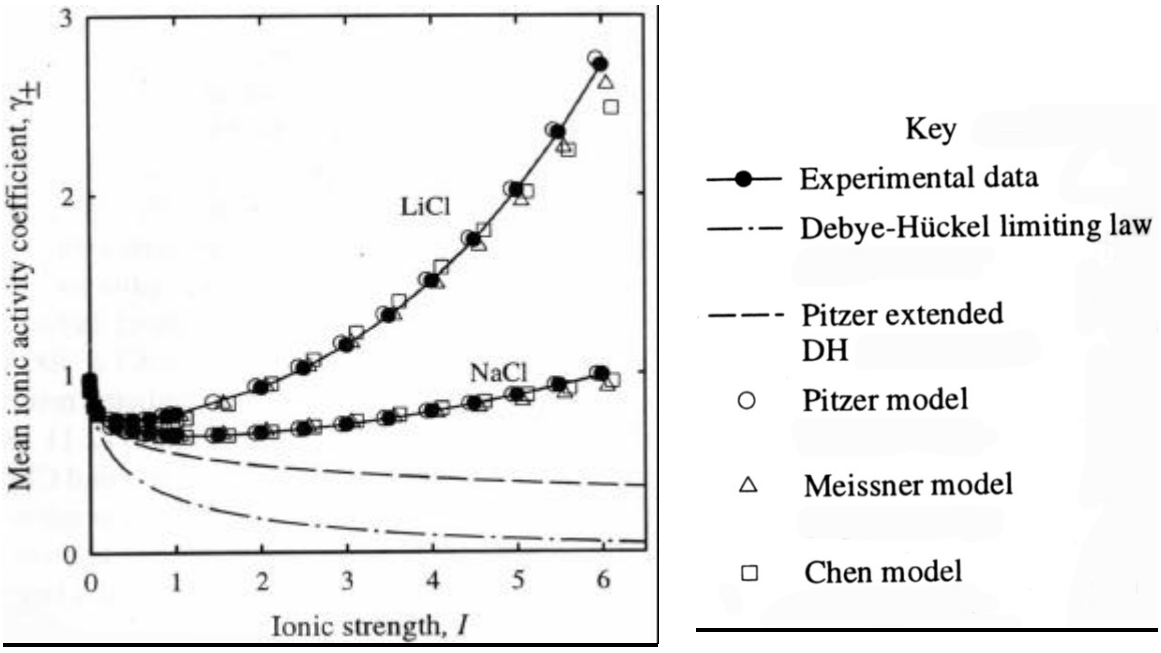

Figure A.1 Example activity coefficient data for the different models

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M.S. in Electrical Engineering, (Expected December 2001)

West Virginia University
B.S. in Computer Engineering (December 1997)

West Virginia University
B.S. in Electrical Engineering(December 1997)

Work Experience:

1997-Present Research and Teaching Assistant at West Virginia University, Morgantown, WV. Research includes electronics work in the virtual reality lab, rebuilding of a evaporation deposition station, microfabrication processing of semiconductor materials, and nano-structure device fabrication. Teaching includes an Digital Signal Processing class, Signal and Systems I class, Electrical Circuit II class, two microprocessor laboratories, one analog laboratory, and the design and teaching of a sensors and displays laboratory.

1997-1998 Director of Research & Development at Interactive Innovations Technologies, Morgantown, WV. Responsibilities include selecting and planning research, finding sources of funding for the research, and performing the research. Author of three SBIR and one STTR proposals.

Summer 1996 Test and design engineer at Sensus Technologies. Work involved designing, developing and testing software and hardware for GPS based water meter systems.

1994-Present Consultant and Accountant at A-One Cleaning Services, Inc., Morgantown, WV. Work involves PC maintenance, job and employee consulting, supervising, laborer, and all aspects of the accounting at the company.

Awards:

Promise Grant for the writing of "Peltier Haptic Interface" SBIR Proposal (July 1998)

Promise Grant for the writing of "Relaxation Pad Musical Interpretation System" SBIR Proposal (July 1998)

Publications:

Journal Papers

1. P. Sines and B. Das, "VRSEMLAB : a low cost virtual reality system to illustrate complex concepts involving spatial relationships", *International J. of Virtual Reality* (in print).

2. C. Garman, P. Sines, S. McGinnis and B. Das, "An improved automated anodization apparatus for fabricating nanostructure devices and porous silicon", *Rev. Scientific. Instruments*, 72, pp. 275-277, 2001.

3. B. Das, S.P. McGinnis and P. Sines, "High efficiency solar cells based on Semiconductor nanostructures", *Solar Energy Materials & Solar Cells*, 63, pp. 117-123, 2000.

4. B. Das and P. Sines, "Peltier haptic interface (PHI) for improved sensation of touch in virtual environment", Virtual Reality 4, pp 260-264, 1999.

5. S. McGinnis, P. Sines and B. Das, "Pulsed current anodization : an effective method for fabricating patterned porous silicon p-n junction light-emitting diodes"; *Electrochemical and Solid State Letters 2*, pp. 468-471 (1999).

Conference Papers

1. P. Sines and M. Long, "Math and Science In Amusement Parks," *West Virginia Conference of Teachers of Mathematics,* Flatwoods, WV, March 2001.

2. B. Das, S. McGinnis, P. Sines, and D. Gray, "Multijunction Solar Cells based on Nanostructure Arrays," *Spring 2001 Electrochemical Society Meeting*, Washington, DC., March 2001.

3. S.P. McGinnis, P. Sines, C. Garman, D. Grey, W. Zhang, and B. Das, "Template Based High Efficiency Nanostructure Photovoltaic Cells", *28th IEEE Photovoltaic Specialist Conference*, Anchorage, AK, Sept. 2000.

4. B. Das, S.P. McGinnis, P. Sines, C. Garman, D. Grey, and W. Zhang, "Nanostructure Arrays for Multijunction Solar Cells", *National Center for Photovoltaics Program Review*, Denver, CO, April 2000.

5. S. P. McGinnis, P. Sines, C. Garman, and B. Das, "Anodization of Silicon Using a Preformed Nanoscale Template", *Microcrystalline and Nanocrystalline Semiconductor Materials and Structures*, 2000 MRS Fall Meeting, Boston, MA, 2000.

6. S. McGinnis, P. Sines and B. Das, "Electrochemical fabrication of semiconductor quantum wires for photovoltaic applications", *3rd International Conference on Low Dimensional Structures and Devices*, Antalya, Turkey, Sept. 1999.

7. C. Allport, B. Schreiner, P. Sines and B. Das; "Education in Three Dimensions: Using Virtual Reality in a Classroom for Illustrating Spatial Relationships", *Proc. International Conference on Engineering Education*, Prague, June 1999.

8. B. Das, S.P. McGinnis, and P. Sines, "A Low Cost High Efficiency Multijunction Photovoltaic Cell Using Electrochemically Fabricated Semiconductor Nanostructures", Proc. of the *Photovoltaics for the 21st Century*, 196th ECS Meeting, Seattle, WA, May 1999.

9. Christopher Allport, Brandon Schreiner, Paul Sines and Biswajit Das; "Virtual Reality Semiconductor Laboratory (VRSEMLAB) : An Advanced Training Tool for Teaching Complex Ideas", *Proc. International Conference on Visual Computing*, Feb. 1999, Goa 1999.

10. C. S. Allport, B. D. Schreiner, and P. B. Sines, Virtual Reality Semiconductor Laboratory, *IEEE 1997 Frontiers in Education Conference Program*, p. 58, Pittsburgh, PA November 1997.

Current Research:

Nano-Structure Based Opto-Electronic Devices

(Master's Thesis Research)

This project involves anodization of Aluminum thin films to create a periodic array of alumina pores on Silicon substrates. These pores will then have layers of p-type and n-type materials deposited in them for the implementation of solar cells and other opto-electronic devices. For my Master's Thesis, my focus was on developing this technique and characterizing the rates of anodizations for various current densities on Silicon, Silicon Carbide, Glass and Platinum substrates.

Sponsored by NREL and DOE.

Teams of Interdisciplinary Graduate fellows Engaged to Reinvigorate Students in science, math, engineering and technology (TIGERS)

(Assistantship)

The TIGERS project is a NSF funded project at West Virginia University to provide professional development to future professors and for current middle school teachers. This past year I worked with four middle schools in the area and co-planned and co-taught with the middle school teachers. Our theme this year was based on an amusement park, on which our lessons in math and science were based. This ranged from looking at and building roller coasters all the way to food stands and entertainment. The teachers learned new techniques as to how to incorporate everyday events more easily into their classrooms, and the fellows learned different classroom management techniques that are applicable to college classrooms. For the upcoming year, I have been promoted to a "Super-fellow". So in addition to the co-planning and co-teaching, I will also have more administrative and managerial duties as well as the responsibility to lead other fellows towards success of the program.

Other Projects:

Peltier Haptic Interface (PHI)

Peltier Haptic Interface (PHI) is an advanced virtual reality glove that will provide improved sensation of touch in virtual environments. PHI will provide force/pressure feedback that can be varied independently on each finger, as well as temperature sensation that can be varied non-uniformly over the whole hand. The combination of these sensations will provide a more realistic sense of touch and significantly increase the realism virtual environments. PHI will find extensive applications in biomedical simulations, teaching, industrial line training, and many other areas.

Virtual Reality Semiconductor Laboratory (VRSemLab)

(Senior Design Project)

My senior design project was to develop VRSEMLAB, a low cost Virtual Reality application to teach the complex subject of semiconductor device physics to undergraduate students. VRSEMLAB demonstrates an effective method for using virtual reality to model complex 3D systems in an experimental environment free of concerns of physical safety, equipment limitations, and size limitations. Based on this project, I have developed a journal paper which has been accepted for publication in the International Journal of Virtual Reality.